CON_ETHERNET
CON_GIGA_ETH.SchDoc
ETHERNET

ETHERNET_PHY
GIGA_ETHERNET_PHY_RT8211F.SchDoc
ETHERNET
RGM2
GMAC0_nRST
GPIO3_B.BIT7

MCU
RK3588S.SchDoc
RGM2
RESET_L
RESET#

PWR3
PWR_5V0 4V0 SYS.SchDoc
EXT_EN
5V_EN
GPIO0_D60.BIT3

PWR1
PWR_PMIC_RK806-1.SchDoc
RESET_L
SPI_CS
SPI_MOSI
SPI_CLK
PWRON_L
INT
CTRL1
CTRL2
CTRL3
EXT_EN
GPIO0_B.BIT1
GPIO0_A.BIT6
GPIO0_A.BIT5
PWRBTN#
GPIO0_A.BIT7
GPIO0_A.BIT2
GPIO0_C.BIT3
GPIO0_C.BIT2

DC_JACK
CON_DCJACK
CON_DCJACK.SchDoc
DC

VCC5V0_SYS

CON_USB3
CON_USB3_RA.SchDoc
CON_USB3-1

USB3-1
USB3_BUS_PWR.SchDoc
EXT
INT
IN
PWREN
GPIO1_A.BIT6

USB3_2
I2S_0
ADC
GPIO0_A
GPIO0_B
GPIO0_C
GPIO0_D60

DDR5_CH0
DDR5_CH0_32bit_315P.SchDoc
DDR_0_A
DDR_0_B

DDR_0_A
DDR_0_B

DDR5_CH1
DDR5_CH0_32bit_315P.SchDoc
DDR_0_A
DDR_0_B

DDR_1_A
DDR_1_B

CON_USB3_TYPEC
CON_USB3.0_TYPEC.SchDoc
CON_TYPEC

USB3-TYPEC
USB3.0_TYPEC.SchDoc
EXT
INT
PWR_EN
INT
SBU1_DC
SBU2_DC
SCL
SDA
GPIO0_A.BIT0
GPIO4_A.BIT5
GPIO4_A.BIT0
GPIO4_A.BIT1
GPIO1_D76.BIT6
GPIO1_D76.BIT7

TYPEC

PWR2
PWR_DCDC_CPU_GPU.SchDoc
I2C2
I2C0
VDD_CPU_FB
PCIE_PWREN
EXT_EN
VSEL2
VSEL3
VSEL6
LCD_PWREN
GPIO0_A.BIT3
GPIO0_C.BIT1
GPIO0_D60.BIT6
GPIO4_A.BIT3

CON_USB2
CON_USB_RA.SchDoc
USB1

USB1
USB_HOST_PWR_SW.SchDoc
EXT1
USB1
USB_POWER
PWREN
GPIO1_C.BIT6

USB2_0

GPIO1_A
GPIO1_B
GPIO1_C
GPIO1_D50
GPIO1_D76

GPIO3_B
GPIO3_C
GPIO3_D50

CON_UART
CON_UART.SchDoc
UART

UART2_M0

CON_HDMI
CON_HDMI.SchDoc
CON

HDMI
HDMI_I2C.SchDoc
HDMI_TX_ON_H
EXT
HDMI
GPIO4_B.BIT6

GPIO4_A
GPIO4_B
HDMI

MIPI_CSI

MIPI_DSI

LCD
CON_LCD_FH34SRJ-30S_MIPI.SchDoc
MIPI_DSI
RST
TOUCH_RST
TOUCH_INT
LED_ANODE
LED_CATHODE
LCD_I2C
GPIO1_B.BIT10
GPIO1_A.BIT4
GPIO1_A.BIT3

BACKLIGHT
BACKLIGHT_SGM3752.SchDoc
LED_ANODE
LED_CATHODE
LCD_PWM
GPIO4_B.BIT2

REV_HISTORY
M2_REV_HISTORY.SchDoc

EMMC
EMMC.SchDoc
SD

eMMC

FAN
CON_FAN.SchDoc
PWM
GPIO1_A.BIT2

T_FLASH
CON_MICROSD_HD08-AL00335.SchDoc
CON
SD_CD
GPIO0_A.BIT4

SD

M.2
CON_M2.SchDoc
PCIE20
PCIE2
M.2_DETn
CLKREQn
RERSTn
WAKEn
GPIO0_C.BIT14
GPIO1_A.BIT0
GPIO1_A.BIT7
GPIO1_A.BIT1

I2C
SDA
SCL
GPIO1_D76.BIT7
GPIO1_D76.BIT6

AUDIO
CON_AUDIO.SchDoc
AUDIO
VIN3_HP_HOOK
PHONE_DET
HP_DET
MIC_IN_P
HPL
HPR
ADC.AIN3
GPIO1_D50.BIT5
HP_DET
MIC_IN_P

AUDIO
CODEC_ES8316.SchDoc
AUDIO
I2S
I2C7
INT
I2S_0
GPIO1_D50.BIT3

I2C
SCL
SDA
GPIO1_D50.BIT0
GPIO1_D50.BIT1

DC_JACK
VCC_3V3
J3
1 2
3 4
5 6
7 8
9 10
11 12
13 14
Header-7x2
HPR
HP_DET
MIC_IN_P
PWRBTN#
GPIO3_C.BIT4
GPIO3_C.BIT6
HPL
RESET#
GPIO3_C.BIT5

VCC_3V3
VCC5V0_SYS
J2
GPIO4_A.BIT7
GPIO4_A.BIT6
GPIO0_D60.BIT0
GPIO3_D50.BIT4
GPIO3_D50.BIT5
GPIO4_B.BIT3
GPIO3_D50.BIT2
GPIO3_D50.BIT1
GPIO3_D50.BIT3
GPIO4_B.BIT0
GPIO1_B.BIT7
GPIO1_B.BIT6
GPIO3_D50.BIT0
GPIO3_C.BIT7
ADC.AIN4
GPIO3_C.BIT0
GPIO3_C.BIT1
GPIO3_B.BIT2
GPIO1_B.BIT2
GPIO1_B.BIT3
GPIO0_D60.BIT4
GPIO0_D60.BIT5
GPIO1_B.BIT4
GPIO4_B.BIT1
GPIO4_B.BIT4
GPIO4_B.BIT5
ADC.AIN5
VCC_1V8_S0
HEADER-20x2_2.5

VCC_3V3_S0
R69 2k F
R70 2k F
GPIO4_B.BIT0
GPIO4_B.BIT1

VCC_3V3_S0
R71 2k F
R72 2k F
GPIO4_A.BIT7
GPIO4_A.BIT6

Mounting Holes

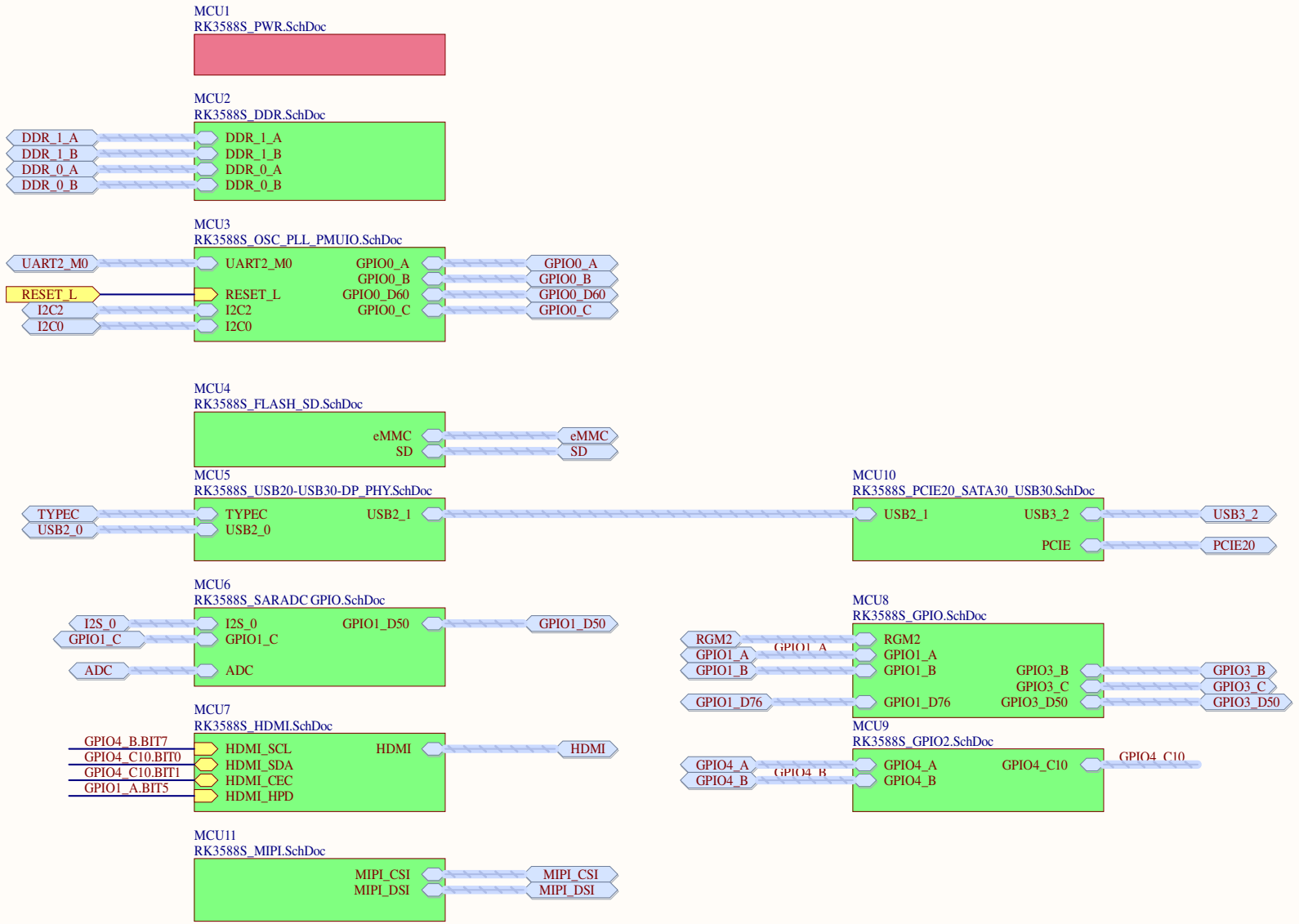
MH1
MOUNTING HOLE 3MM
MH2
MOUNTING HOLE 3MM
MH3
MOUNTING HOLE 3MM
MH4
MOUNTING HOLE 3MM

RTC
RTC_PCF8663.SchDoc
INT
SDA
SCL
CLKOUT
GPIO0_B.BIT0
GPIO1_D76.BIT7
GPIO1_D76.BIT6
GPIO0_B.BIT2

H1 Heat Sink
Heat_Sink_55mm
40x40x12_wFANontop

M2_LEDS
M2_LEDS.SchDoc
PWRBTN#
RESET#
PWRON_L
RESET_L
PWR-LED
SYS_LED
GPIO1_B.BIT5
GPIO1_B.BIT1

Title	M2-MAIN		
Size: A3	Number: 1	Revision: 1.0	Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Date: 2024-07-29	Time: 오후 4:15:42	Sheet 1 of 41	
File: M2-MAIN.SchDoc		Designed by: ruppi.kim@hardkernel.com	



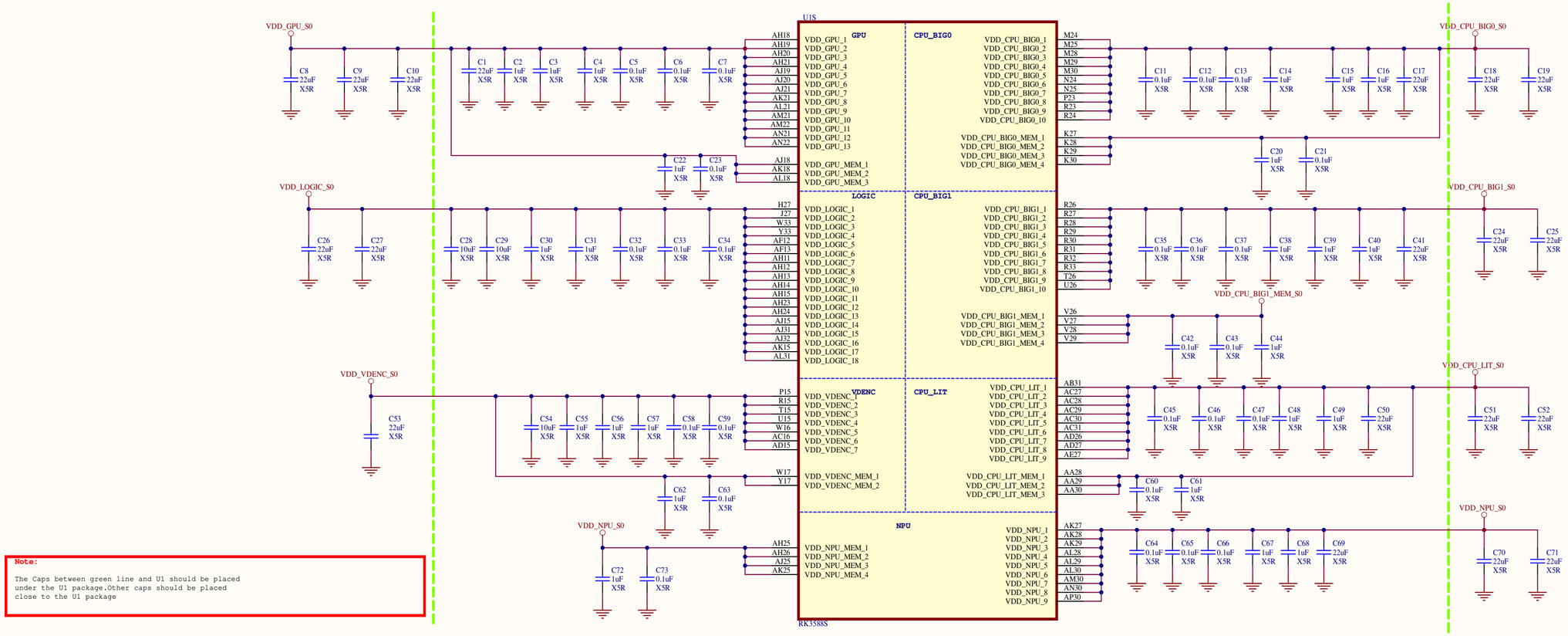
Title	*MCU RK3588S*		
Size: A4	Number: 3	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:42	Sheet 2 of 41	
File: RK3588S.SchDoc			

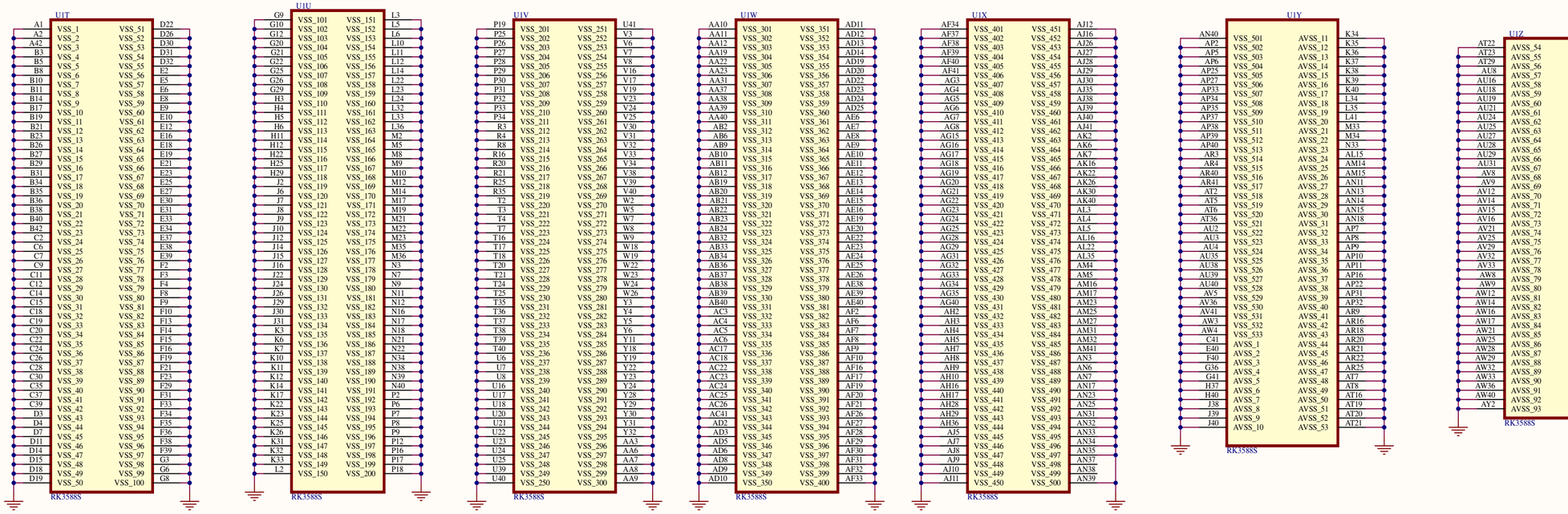
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: neal.kim@hardkernel.com

ODROID

RK3588S(Power&Gnd)



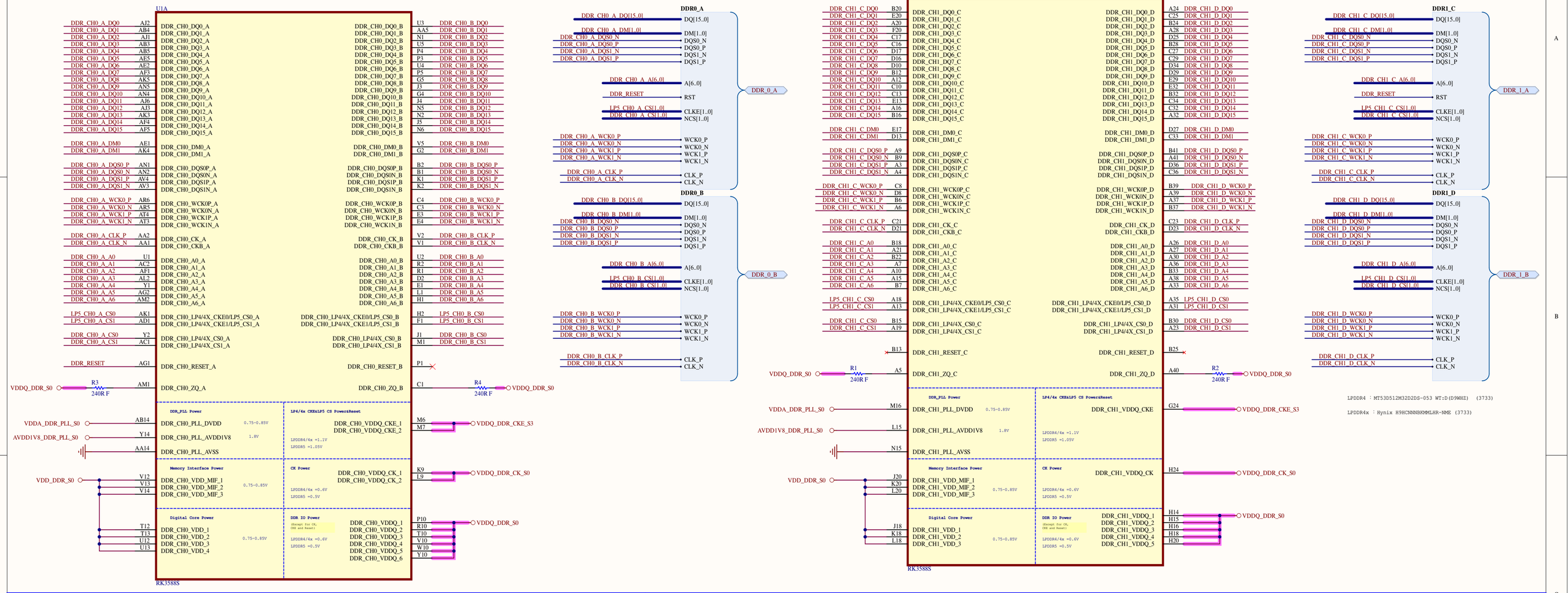


Title	RK3588S POWER/GND		
Size: A2	Number: 2	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:43	Sheet 3 of 41	
File: RK3588S_PWR.SchDoc		Designed by: neal.kim@hardkernel.com	

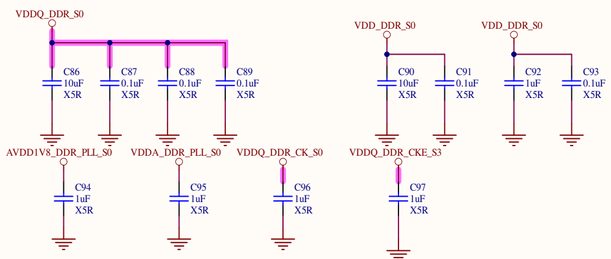
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

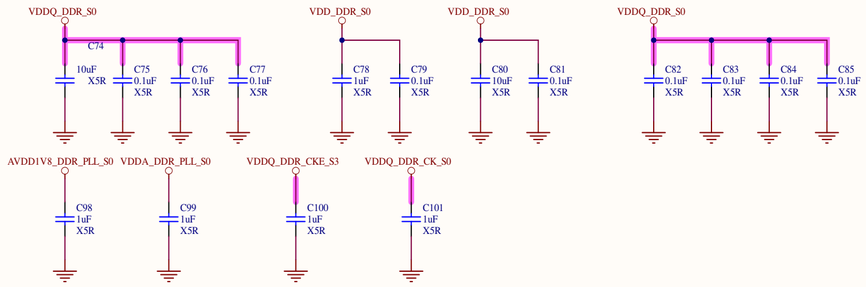
ODROID

RK3588S(DDR PHY)



DDR FILTER





Title	RK3588S DDR PHY			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A2	Number: 12	Revision: 0.1			
Date: 2024-07-29	Time: 오후 4:15:43	Sheet 4 of 41			
File: RK3588S_DDR.SchDoc				Designed by: neal.kim@hardkernel.com	

RK3588S(OSC/PLL/PMUIO1)

Note:

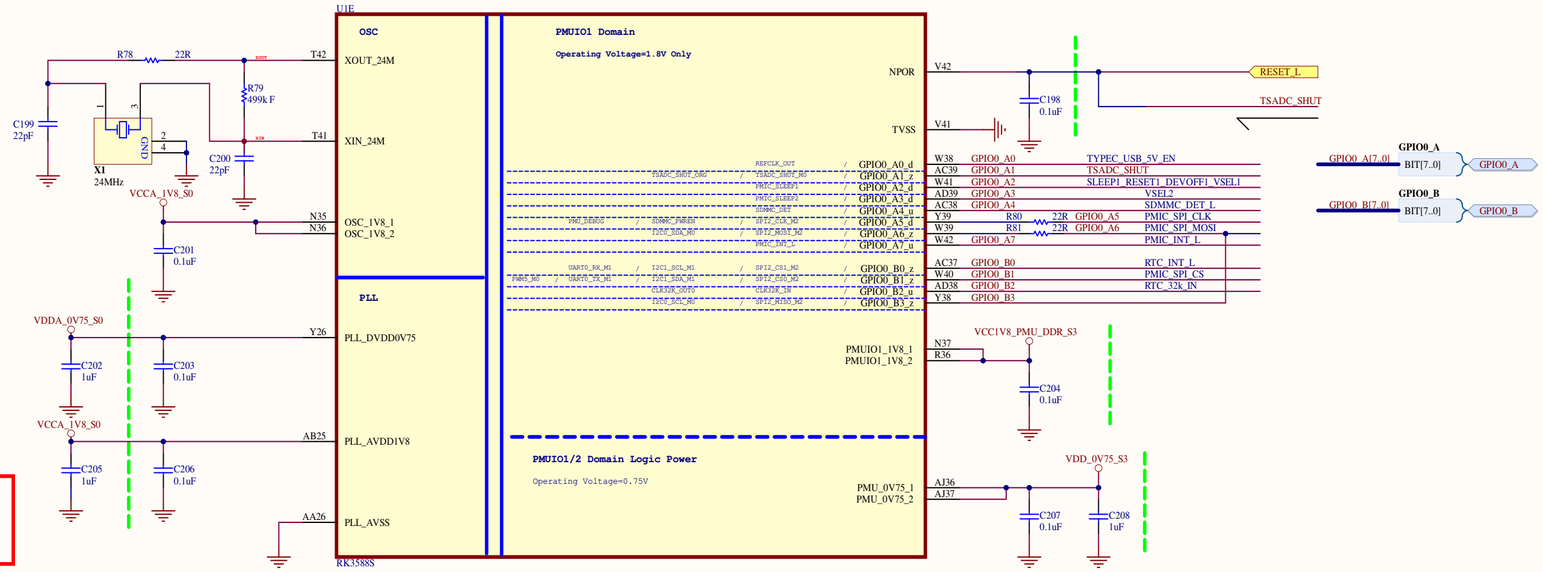
Adjusted the load capacitance
according to the crystal specification

The CL is the load capacitance of
the crystal that is recommended by
the crystal vendors to obtain
target clock frequency.

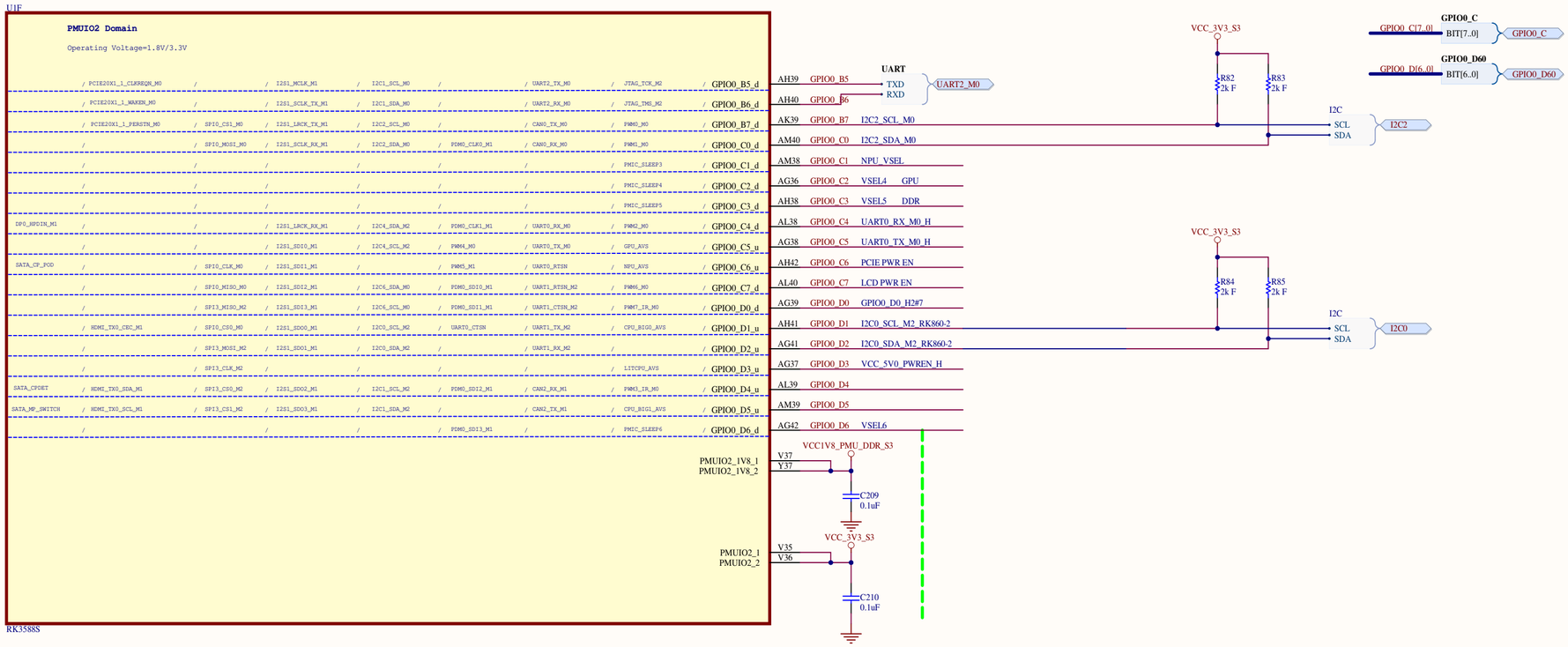
CL=(CL1*CL2/(CL1+CL2))+PCB strays
Total CL<=12pF

Note:

The Caps between green line and U1000 should be
placed under the U1000 package.Other caps should
be placed close to the U1000 package

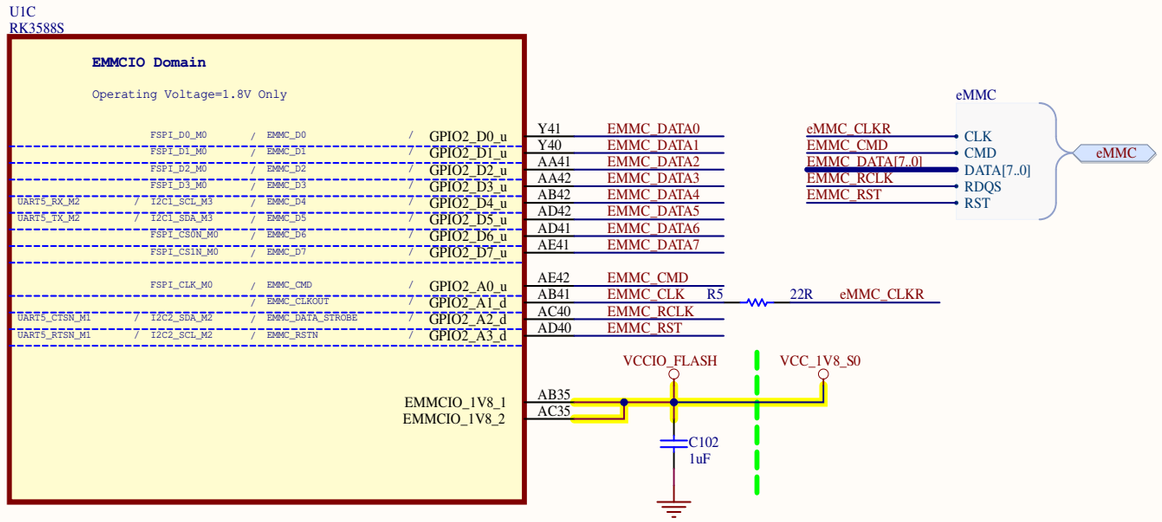


RK3588S(PMUIO2)

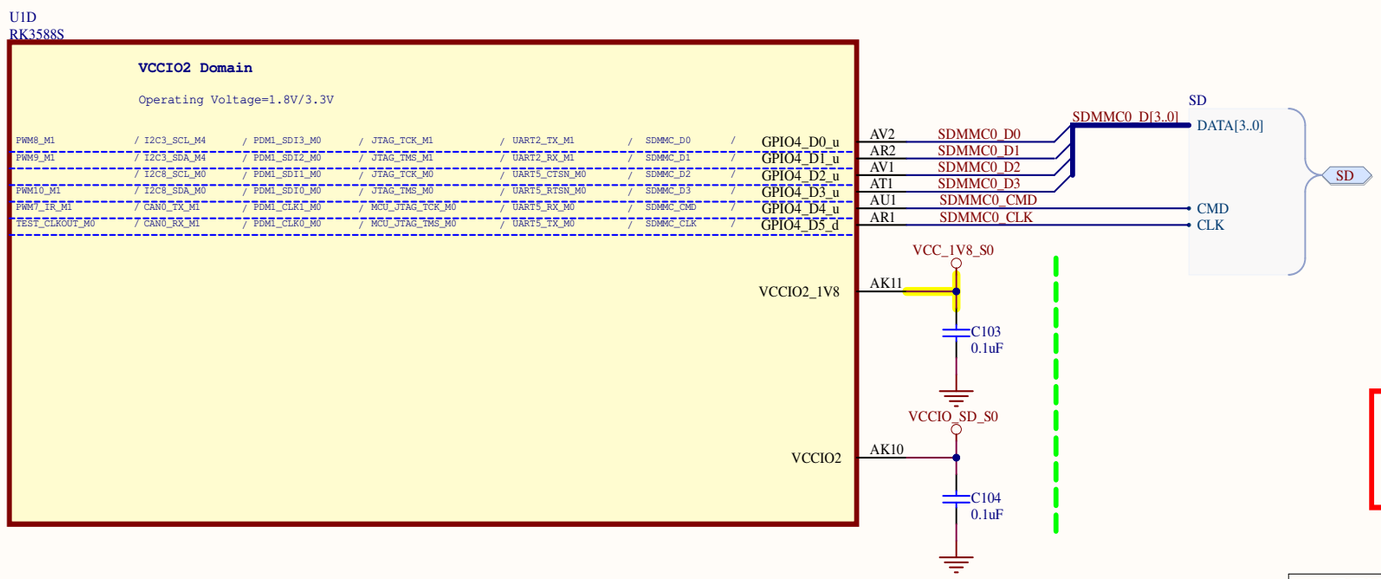


Title	RK3588S OSC/PLL/PMUIO				Hardkernel Co.,LTD. 475-1 Manamro Manangu, Anyang City Gyeonggido South Korea
Size:	A2	Number:	13	Revision:	0.1
Date:	2024-07-29	Time:	오후 4:15:44	Sheet	5 of 41
File:	RK3588S_OSC_PLL_PMUIO.SchDoc			Designed by:	neal.kim@hardkernel.com

RK3588S(EMMCIO Domain)



RK3588S(VCCIO2 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

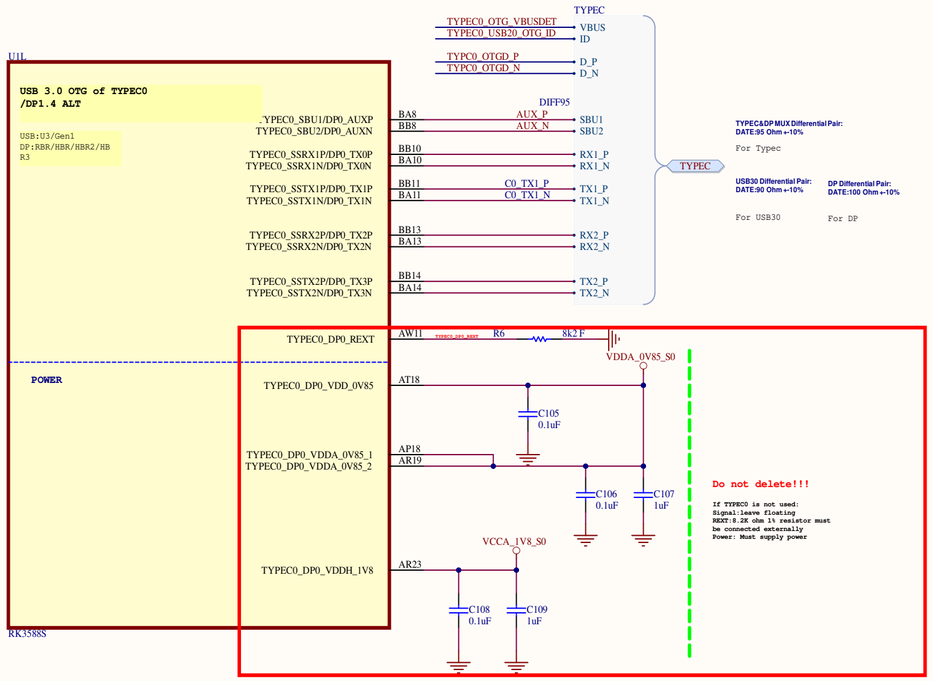
Title	*RK3568 FLASH SD Controller*		*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A3	Number: 14	Revision: 0.1	ODROID
Date: 2024-07-29	Time: 오후 4:15:44	Sheet 6 of 41	
File: RK3588S_FLASH_SD.SchDoc		Designed by: neal.kim@hardkernel.com	

RK3588S(USB3.0/DP1.4)

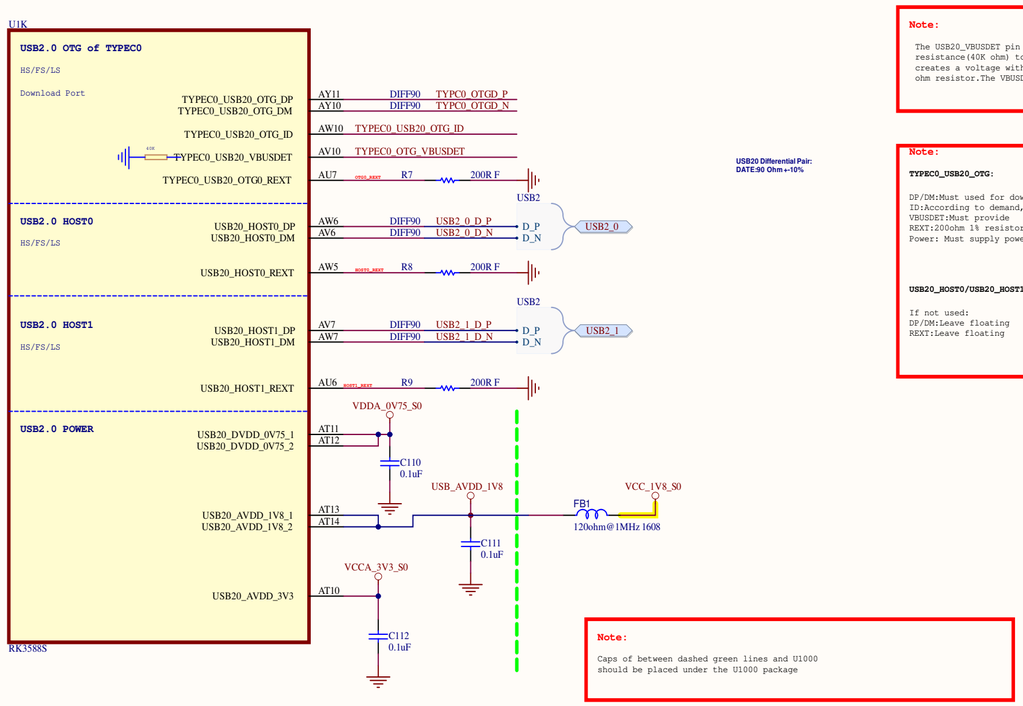
USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0~3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N* *SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N* *DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



RK3588S(USB2.0)



Note:

The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

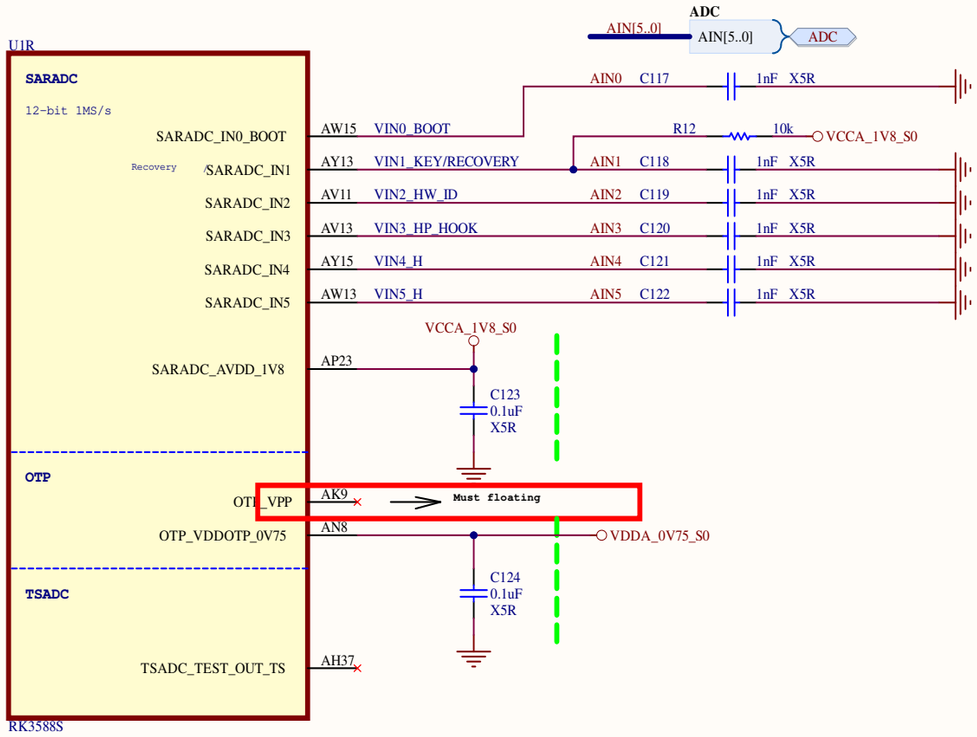
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:

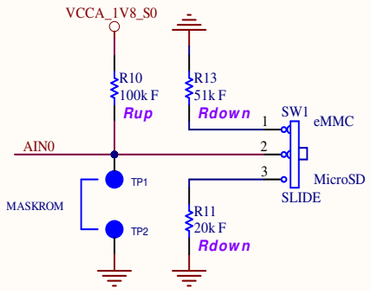
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Title	*RK3588S_USB20/USB30//DP PHY*			*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A2	Number: 15	Revision: 0.1		
Date: 2024-07-29	Time: 오후 4:15:44	Sheet 7 of 41		
File: RK3588S_USB20-USB30-DP_PHY.SchDoc			Designed by: neal.kim@hardkernel.com	

RK3588S(SARADC/OTP/TSADC)

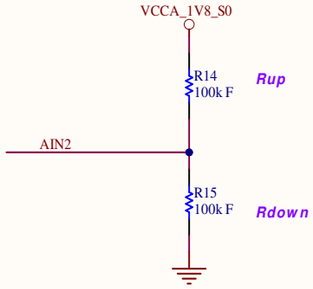


BOOT MODE CONFIG



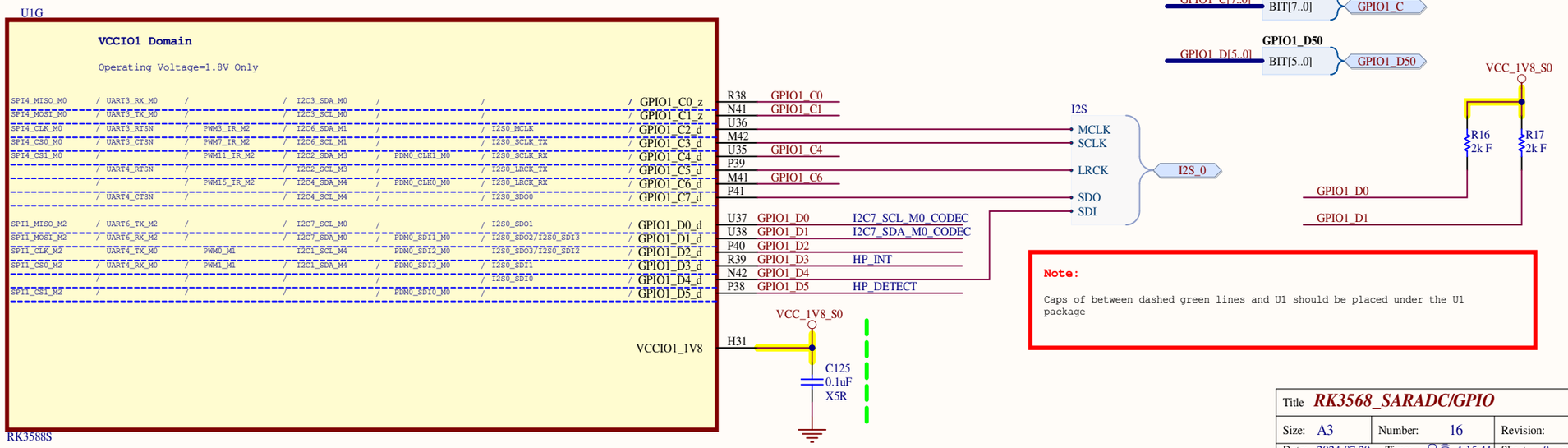
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S(VCCIO1 Domain)



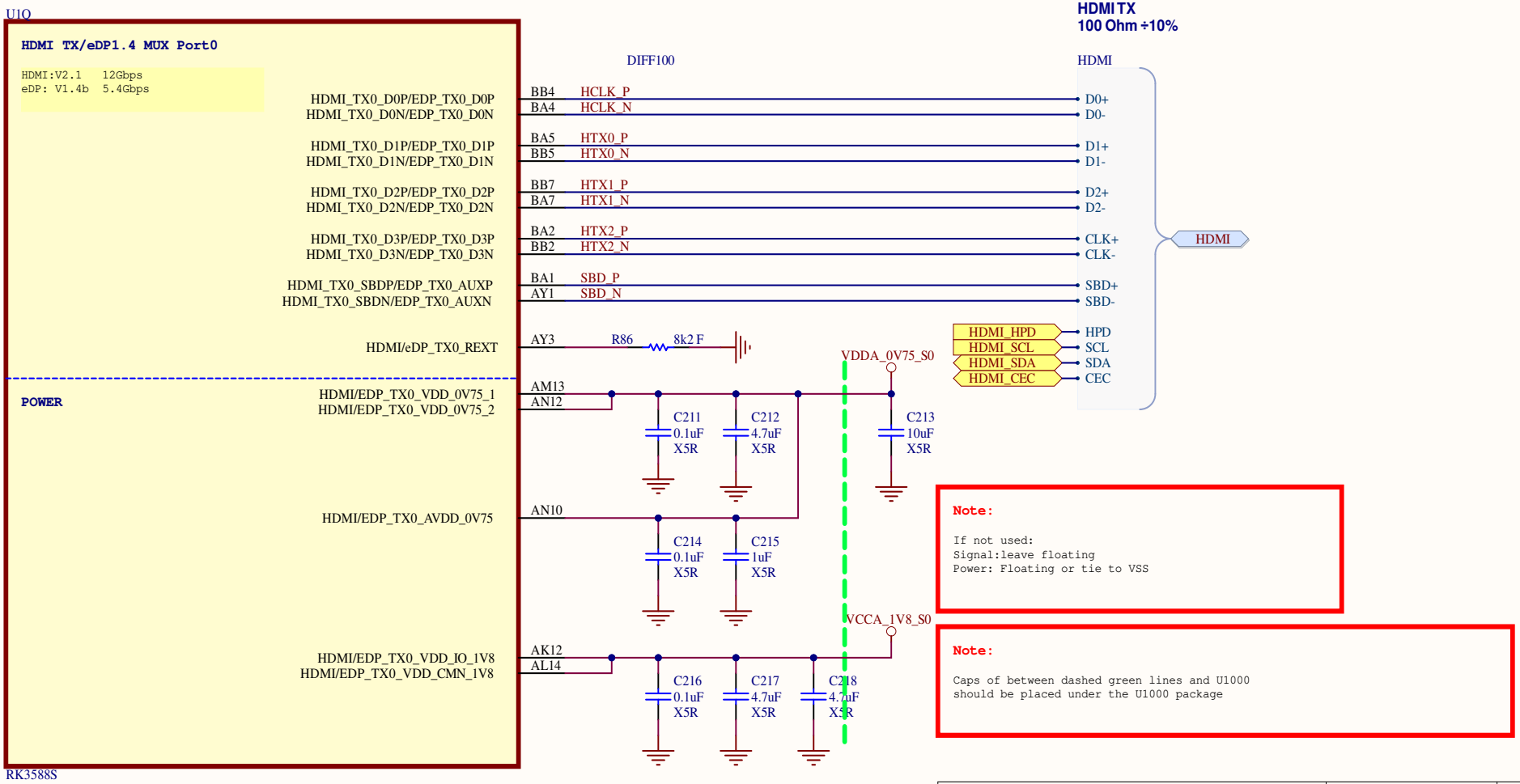
Title	RK3568_SARADC/GPIO		Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Size: A3	Number: 16	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:44	Sheet 8 of 41	
File: RK3588S_SARADC GPIO.SchDoc		Designed by: neal.kim@hardkernel.com	

ODROID

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:

If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package

Title	*RK3588_HDMI*		
Size: A4	Number: 17	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:44	Sheet 9 of 41	
File: RK3588S_HDMI.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: neal.kim@hardkernel.com

ODROID

RK3588S(VCCIO4 Domain)

U1H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	PCIE20X1_1_CLKREQn_M2	DP0_HPDIN_M2	UART6_RX_M1	SPI4_MISO_M2	I2C2_SDA_M4	GPIO1_A0_d
	PCIE20X1_1_WAKEn_M2		UART6_TX_M1	SPI4_MOSI_M2	I2C2_SCL_M4	GPIO1_A1_d
PWM0_M2		VOP_POST_EMPTY	UART6_RTSN_M1	SPI4_CLK_M2	I2C4_SDA_M3	GPIO1_A2_d
PWM1_M2			UART6_CTSN_M1	SPI4_CS0_M2	I2C4_SCL_M3	GPIO1_A3_d
				SPI2_MISO_M0		GPIO1_A4_d
		HDMI_TX0_HPD_M0		SPI2_MOSI_M0		GPIO1_A5_d
				SPI2_CLK_M0		GPIO1_A6_d
PWM3_IR_M3	PCIE20X1_1_PERSTn_M2			SPI2_CS0_M0	PDM1_SDI0_M3	GPIO1_A7_u
				SPI2_CS1_M0	PDM1_SDI1_M1	GPIO1_B0_u
				SPI0_MISO_M2	PDM1_SDI2_M1	GPIO1_B1_d
			UART4_RX_M2	SPI0_MOSI_M2	PDM1_SDI3_M1	GPIO1_B2_d
	SATA0_ACT_LED_M1		UART4_TX_M2	SPI0_CLK_M2	PDM1_CLK1_M1	GPIO1_B3_d
			UART7_RX_M2	SPI0_CS0_M2	PDM1_CLK0_M1	GPIO1_B4_u
			UART7_TX_M2	SPI0_CS1_M2		GPIO1_B5_u
		MIPI_CAMERA1_CLK_M0	UART1_TX_M1	SPDIF0_TX_M0	I2C5_SCL_M3	GPIO1_B6_u
PWM13_M2	SATA2_ACT_LED_M1	MIPI_CAMERA2_CLK_M0	UART1_RX_M1	SPDIF1_TX_M0	I2C5_SDA_M3	GPIO1_B7_u
PWM14_M2		MIPI_CAMERA3_CLK_M0	UART1_RTSN_M1		I2C8_SCL_M2	GPIO1_D6_u
PWM15_IR_M3		MIPI_CAMERA4_CLK_M0	UART1_CTSN_M1		I2C8_SDA_M2	GPIO1_D7_u

G40	GPIO1_A0	PCIE20x1_1_CLKREQn_M0	
L40	GPIO1_A1	PCIE20x1_1_WAKEn_M0	
D38	GPIO1_A2	FAN_PWM	
L39	GPIO1_A3	TOUCH_INT_L	
G37	GPIO1_A4	TOUCH_RST_L	
M40	GPIO1_A5	HDMI_TX0_HPD_M0	
D39	GPIO1_A6	USB3_PWR_EN_H	
H38	GPIO1_A7	PCIE20x1_1_PERSTn_M0	
H39	GPIO1_B0	GPIO1_B_0_H	
G39	GPIO1_B1	PWR_LED	
M38	GPIO1_B2	GPIO1_B_2_H	
M37	GPIO1_B3	GPIO1_B_3_H	
M39	GPIO1_B4	GPIO1_B_4_H	
D40	GPIO1_B5	SYS_LED	
L38	GPIO1_B6	GPIO1_B_6_H#31	
F37	GPIO1_B7	GPIO1_B_7_H#29	
L37	GPIO1_D6	DSI_I2C_SCL	
G38	GPIO1_D7	DSI_I2C_SDA	

VCCIO4_1V8_1
VCCIO4_1V8_2
G27
G28

VCCIO4
G31

VCC_1V8_S0
C219
0.1uF
X5R

VCC_3V3_S0
C220
0.1uF
X5R

RK3588S

GPIO1_A[7..0] → BIT[7..0] **GPIO1_A** → GPIO1_A

GPIO1_B[7..0] → BIT[7..0] **GPIO1_B** → GPIO1_B

GPIO1_D[7..6] → BIT[7..6] **GPIO1_D76** → GPIO1_D76

VCC_3V3_S0
R87 2k F
R88 2k F
GPIO1_D6
GPIO1_D7

RK3588S(VCCIO5 Domain)

U1H

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	PWM10_M0	SPI4_MISO_M1	I2C6_SDA_M4	GMAC1_TXD2	I2S3_MCLK	FSPI_D0_M2	SDIO_D0_M1	GPIO3_A0_u
AUDDSM_LN	PWM11_IR_M0	SPI4_MOSI_M1	I2C6_SCL_M4	GMAC1_TXD3	I2S3_SCLK	FSPI_D1_M2	SDIO_D1_M1	GPIO3_A1_u
AUDDSM_LP	UART8_TX_M1	SPI4_CLK_M1		GMAC1_RXD2	I2S3_LRCK	FSPI_D2_M2	SDIO_D2_M1	GPIO3_A2_u
AUDDSM_RN	UART8_RX_M1	SPI4_CS0_M1		GMAC1_RXD3	I2S3_SDO	FSPI_D3_M2	SDIO_D3_M1	GPIO3_A3_u
AUDDSM_RP	UART8_RTSN_M1	SPI4_CS1_M1		GMAC1_TXCLK	I2S3_SDI		SDIO_CMD_M1	GPIO3_A4_d
	UART8_CTSN_M1		I2C4_SDA_M0	GMAC1_RXCLK	FSPI_CLK_M2	MIPI_CAMERA0_CLK_M1	SDIO_CLK_M1	GPIO3_A5_d
			I2C4_SCL_M0	ETH1_REFCLKO_25M		MIPI_CAMERA1_CLK_M1		GPIO3_A6_d
				GMAC1_RXD0		MIPI_CAMERA2_CLK_M1	PWM8_M0	GPIO3_A7_u
				GMAC1_RXD1	I2S2_SCLK_RX_M1	MIPI_CAMERA3_CLK_M1	PWM9_M0	GPIO3_B0_u
	UART2_TX_M2			GMAC1_RXDV_CRS	I2S2_LRCK_RX_M1	MIPI_CAMERA4_CLK_M1	PWM2_M1	GPIO3_B1_d
	UART2_RX_M2			GMAC1_TXER	I2S2_SDI_M1		PWM3_IR_M1	GPIO3_B2_d
	UART2_RTSN			GMAC1_TXD0	I2S2_SDO_M1			GPIO3_B3_u
	UART2_CTSN			GMAC1_TXD1	I2S2_MCLK_M1			GPIO3_B4_u
	UART3_TX_M1		CAN1_RX_M0	GMAC1_TXEN	I2S2_SCLK_TX_M1		PWM12_M0	GPIO3_B5_u
	UART3_RX_M1		CAN1_TX_M0	GMAC1_MCLKINOUT	I2S2_LRCK_TX_M1		PWM13_M0	GPIO3_B6_d
		SPI1_MOSI_M1	I2C3_SCL_M1	GMAC1_PTP_REF_CLK				GPIO3_B7_d
	UART7_TX_M1	SPI1_MISO_M1	I2C3_SDA_M1	GMAC1_PPSTRIG				GPIO3_C0_d
	UART7_RX_M1	SPI1_CLK_M1		GMAC1_PPSCLK				GPIO3_C1_d
	UART7_RTSN_M1	SPI1_CS0_M1	I2C8_SCL_M4	GMAC1_MDC		MIPI_TE0	PWM14_M0	GPIO3_C2_d
	UART7_CTSN_M1	SPI1_CS1_M1	I2C8_SDA_M4	GMAC1_MDIO		MIPI_TE1	PWM15_IR_M0	GPIO3_C3_d
	UART5_TX_M1	SPI3_CS0_M3	CAN2_RX_M0	CIF_D8		FSPI_CS0N_M2		GPIO3_C4_u
	UART5_RX_M1	SPI3_CS1_M3	CAN2_TX_M0	CIF_D9		FSPI_CS1N_M2		GPIO3_C5_u
		SPI3_MISO_M3		CIF_D10				GPIO3_C6_u
		SPI3_MOSI_M3	I2C5_SCL_M0	CIF_D11	PCIE20X1_2_CLKREQN_M0	HDMI_TX0_SCL_M2		GPIO3_C7_u
	UART4_RX_M1	SPI3_CLK_M3	I2C5_SDA_M0	CIF_D12	PCIE20X1_2_WAKEN_M0	HDMI_TX0_SDA_M2	PWM8_M2	GPIO3_D0_u
	UART4_TX_M1	SPI0_MISO_M3		CIF_D13	PCIE20X1_2_PERSTN_M0		PWM9_M2	GPIO3_D1_d
	UART9_RTSN_M2	SPI0_MOSI_M3	I2C7_SCL_M2	CIF_D14				GPIO3_D2_d
	UART9_CTSN_M2	SPI0_CLK_M3	I2C7_SDA_M2	CIF_D15			PWM10_M2	GPIO3_D3_d
	UART9_RX_M2	SPI0_CS0_M3		MCU_JTAG_TCK_M1		HDMI_TX0_HPD_M1		GPIO3_D4_d
	UART9_TX_M2	SPI0_CS1_M3		MCU_JTAG_TMS_M1			PWM11_IR_M3	GPIO3_D5_d

AR38			TXD2
AR37			TXD3
AT38			RXD2
AT40			RXD3
AT39			TXCLK
AV38			RXCLK
AV37			REFCLKO_25M
AT37			RXD0
AR39	GPIO3_B0		RXD1
AV39	GPIO3_B1		RXDV_CRS
AW34	GPIO3_B2	PWM3_IR_M1_H#12	
AW35	GPIO3_B3		TXD0
AV35	GPIO3_B4		TXD1
AY35	GPIO3_B5		TXEN
AW37	GPIO3_B6		MCLKINOUT
AY34	GPIO3_B7	GMAC1_RSTn	
AR36	GPIO3_C0	UART7_TX_M1_H#8	
AW38	GPIO3_C1	UART7_RX_M1_H#10	
AV40	GPIO3_C2		MDIC
AW39	GPIO3_C3		MDIO
AU34	GPIO3_C4	GPIO3_C4_H2#11	
AV34	GPIO3_C5	GPIO3_C5_H2#12	
AV30	GPIO3_C6	GPIO3_C5_H2#13	
AU30	GPIO3_C7	GPIO3_C7_H#33	
AW31	GPIO3_D0	GPIO3_D1_H#35	
AY27	GPIO3_D1	GPIO3_D1_H#21	
AY30	GPIO3_D2	GPIO3_D2_H#19	
AY31	GPIO3_D3	GPIO3_D1_H#23	
AV31	GPIO3_D4	GPIO3_D4_H#24	
AW30	GPIO3_D5	GPIO3_D5_H#22	

RGM2 → RGM2

RESERVED
AF35
VCCIO5_1V8
AF36

VCCIO5_1
VCCIO5_2
AC33
AC34

VCCIO5_1V8
VCC_1V8_S0
C221
0.1uF
X5R

VCCIO5
VCC_3V3_S0
C222
0.1uF
X5R

RK3588S

GPIO3_B[7..0] → BIT[7..0] **GPIO3_B** → GPIO3_B

GPIO3_C[7..0] → BIT[7..0] **GPIO3_C** → GPIO3_C

GPIO3_D[5..0] → BIT[5..0] **GPIO3_D50** → GPIO3_D50

Note:

Caps of between dashed green lines and U1 should be placed under the U1 package

Title	RK3568_VO Interface2		Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Size: A2	Number: 18	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:45	Sheet 10 of 41	
File: RK3588S_GPIO.SchDoc		Designed by: ruppi.kim@hardkernel.com	

RK3588S(VCCIO6 Domain)

U1J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

BT1120_D0	CIF_D0		I2S1_MCLK_M0	UART9_RTSN_M1	SPI0_MISO_M1			PCIE20X1_1_CLKREQN_M1	GPIO4_A0_d
BT1120_D1	CIF_D1		I2S1_SCLK_TX_M0	UART9_CTSN_M1	SPI0_MOSI_M1			PCIE20X1_1_WAKEN_M1	GPIO4_A1_d
BT1120_D2	CIF_D2		I2S1_LRCK_TX_M0		SPI0_CLK_M1			PCIE20X1_1_PERSTN_M1	GPIO4_A2_d
BT1120_D3	CIF_D3		I2S1_SCLK_RX_M0	UART0_TX_M2					GPIO4_A3_d
BT1120_D4	CIF_D4		I2S1_LRCK_RX_M0	UART0_RX_M2	SPI2_MISO_M1	I2C3_SCL_M2			GPIO4_A4_d
BT1120_D5	CIF_D5		I2S1_SDI0_M0	UART3_TX_M2	SPI2_MOSI_M1	I2C3_SDA_M2			GPIO4_A5_d
BT1120_D6	CIF_D6		I2S1_SDI1_M0	UART3_RX_M2	SPI2_CLK_M1	I2C5_SCL_M2			GPIO4_A6_d
BT1120_D7	CIF_D7		I2S1_SDI2_M0		SPI2_CS0_M1	I2C5_SDA_M2			GPIO4_A7_d
BT1120_CLKOUT	CIF_CLKIN		I2S1_SDI3_M0	UART8_TX_M0	SPI2_CS1_M1	I2C6_SDA_M3			GPIO4_B0_d
SPDIF1_TX_M1	MIPI_CAMERA0_CLK_M0	SATA2_ACT_LED_M0	I2S1_SDO0_M0	UART8_RX_M0	SPI0_CS1_M1	I2C6_SCL_M3			GPIO4_B1_u
CAN1_RX_M1 / BT1120_D8	CIF_HREF	PWM14_M1	I2S1_SDO1_M0	UART8_RTSN_M0	SPI0_CS0_M1	I2C7_SCL_M3		PCIE20X1_1_BUTTON_RSTN	GPIO4_B2_u
CAN1_TX_M1 / BT1120_D9	CIF_VSYNC	PWM15_IR_M1	I2S1_SDO2_M0	UART8_CTSN_M0		I2C7_SDA_M3		PCIE20X1_2_BUTTON_RSTN	GPIO4_B3_u
BT1120_D10	CIF_CLKOUT	PWM11_IR_M1	I2S1_SDO3_M0	UART9_TX_M1			DP0_HPDIN_M0	SPDIF0_TX_M1	GPIO4_B4_u
BT1120_D11		PWM12_M1		UART9_RX_M1	SPI3_MISO_M1				GPIO4_B5_d
BT1120_D12		PWM13_M1			SPI3_MOSI_M1	I2C5_SCL_M1		SATA0_ACT_LED_M0	GPIO4_B6_d
BT1120_D13			HDMI_TX0_SCL_M0		SPI3_CLK_M1	I2C5_SDA_M1		PCIE20X1_2_CLKREQN_M1	GPIO4_B7_u
BT1120_D14			HDMI_TX0_SDA_M0		SPI3_CS0_M1	I2C8_SCL_M3		PCIE20X1_2_WAKEN_M1	GPIO4_C0_u
BT1120_D15	SPDIF1_TX_M2	PWM6_M1	HDMI_TX0_CEC_M0		SPI3_CS1_M1	I2C8_SDA_M3		PCIE20X1_2_PERSTN_M1	GPIO4_C1_d

Note:
BT1120 Only Support Output

VCCIO6_1V8

VCCIO6_1
VCCIO6_2

RK3588S

AV19 GPIO4_A0 TYPEC0_SBU1_DC
AW18 GPIO4_A1 TYPEC0_SBU2_DC
AV26 GPIO4_A2
AY19 GPIO4_A3 LCD_PWREN_H
AW19 GPIO4_A4
AU15 GPIO4_A5 TYPEC0_CC_INT_L
AV18 GPIO4_A6 I2C5_SCL_M3_H
AW26 GPIO4_A7 I2C5_SDA_M3_H
AW27 GPIO4_B0 GPIO4_B0_H#27
AU22 GPIO4_B1 GPIO4_B1_H#28
AT15 GPIO4_B2 LCD_BL_PWM14_M1
AV23 GPIO4_B3 GPIO4_B3_H#15
AV27 GPIO4_B4 UART9_TX_M1_H
AU23 GPIO4_B5 UART9_RX_M1_H
AW22 GPIO4_B6 HDMI_TX0_ON_H
AV22 GPIO4_B7 HDMI_TX0_SCL_M0
AW23 GPIO4_C0 HDMI_TX0_SDA_M0
AY26 GPIO4_C1 HDMI_TX0_CEC_M0

VCC_1V8_S0
AJ34
C312 0.1uF X5R

VCC_3V3_S0
AL33
AM33
C313 0.1uF X5R

GPIO4_A_4_H

GPIO4_A
GPIO4_A[7..0] BIT[7..0] GPIO4_A

GPIO4_B
GPIO4_B[7..0] BIT[7..0] GPIO4_B

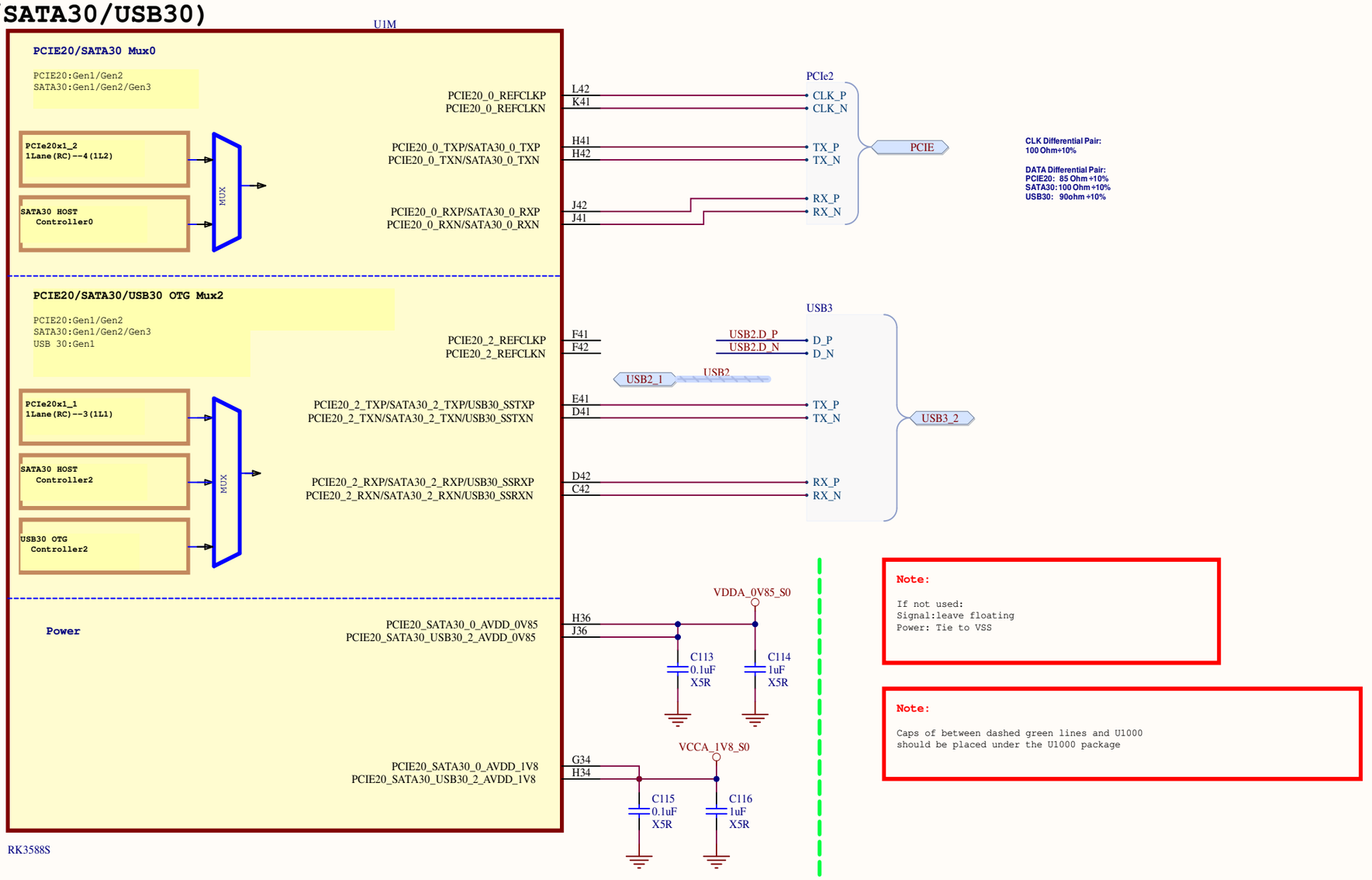
GPIO4_C10
GPIO4_C[1..0] BIT[1..0] GPIO4_C10

Note:

Caps of between dashed green lines and U1
should be placed under the U1 package

Title: RK3588S_GPIO2			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Size: A3	Number: 19	Revision: *	ODROID
Date: 2024-07-29 Time: 오후 4:15:45	Sheet 11 of 41		
File: RK3588S_GPIO2.SchDoc		Designed by: neal.kim@hardkernel.com	

RK3588S(PCIE20/SATA30/USB30)



Note:

If not used:
Signal:leave floating
Power: Tie to VSS

Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Title	RK3568_Audio Interface		Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Size: A3	Number: 20	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:45	Sheet 12 of 41	
File: RK3588S_PCIE20_SATA30_USB30.SchDoc		Designed by: neal.kim@hardkernel.com	

RK3588S(MIPI_DPHY CSI0 RX)

U1N

MIPI DPHY CSI_RX Port0

MIPI V1.2
2.5Gbps

MIPI_CSI0_CLK0P	AN42
MIPI_CSI0_CLK0N	AN41
MIPI_CSI0_D0P	AL42
MIPI_CSI0_D0N	AL41
MIPI_CSI0_D1P	AK41
MIPI_CSI0_D1N	AK42
MIPI_CSI0_CLK1P	AU41
MIPI_CSI0_CLK1N	AU42
MIPI_CSI0_D2P	AT41
MIPI_CSI0_D2N	AT42
MIPI_CSI0_D3P	AP42
MIPI_CSI0_D3N	AP41
MIPI_CSI0_AVCC0V75	AM37
MIPI_CSI0_AVCC1V8	AM35

RK3588S

Note:

If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1*	*x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1* *+* *Sensor2*	*x2Lane* *x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:

When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)

U1Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V1.2
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	BB34
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	BA34
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	BB31
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	BA31
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	BA32
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	BB32
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	BA35
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	BB35
MIPI_DPHY0_TX_D3P/NO_USE	BB37
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	BA37

DIFF100

MIPI_DSI: CLK_P, CLK_N, D0_P, D0_N, D1_P, D1_N, D2_P, D2_N, D3_P, D3_N

MIPI DPHY Differential Pair:
100 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	BB41
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	BA41
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	BA38
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	BB38
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	BA40
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AY40
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AY42
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	BA42
MIPI_DPHY0_RX_D3P/NO_USE	AW41
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AW42

Power

MIPI_D/C_PHY0_VREG	AT33
MIPI_D/C_PHY0_VDD	AR33
MIPI_D/C_PHY_VDD_1V2_1	AR34
MIPI_D/C_PHY_VDD_1V8_1	AR30

C328 1uF X5R

VDDA_0V75_S0

C329 1uF X5R

C330 0.1uF X5R

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

VDDA_1V2_S0

C331 0.1uF X5R

VCCA_1V8_S0

C332 0.1uF X5R

RK3588S

Note:

If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)

U1P

MIPI D/C-PHY DSI_TX Port1

D-PHY:V1.2
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	BB19
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	BA19
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	BB16
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	BA16
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	BA17
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	BB17
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	BA20
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	BB20
MIPI_DPHY1_TX_D3P/NO_USE	BB22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	BA22

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	BA26
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	BB26
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	BA23
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	BB23
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	BB25
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	BA25
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	BB28
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	BA28
MIPI_DPHY1_RX_D3P/NO_USE	BA29
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	BB29

Power

MIPI_D/C_PHY1_VREG	AT27
MIPI_D/C_PHY1_VDD	AR27
MIPI_D/C_PHY_VDD_1V2_2	AR35
MIPI_D/C_PHY_VDD_1V8_2	AT30

RK3588S

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

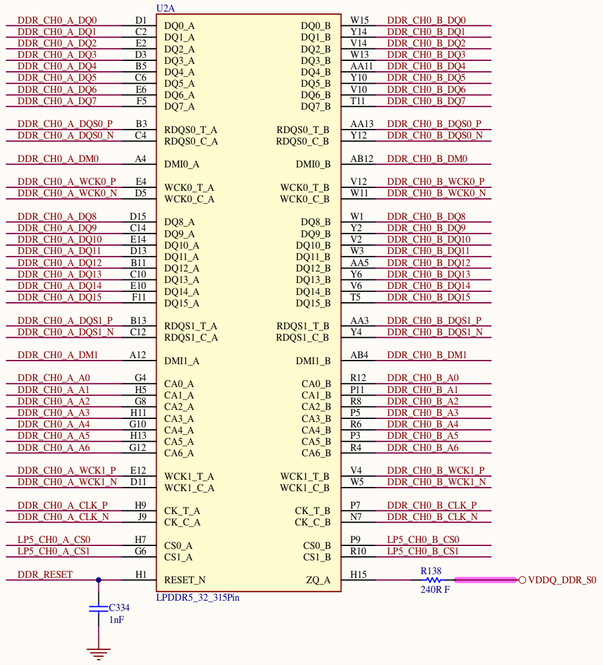
Note:

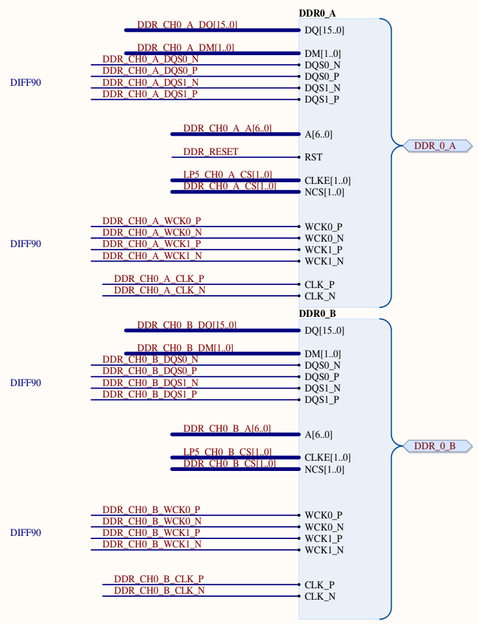
If not used:
Signal:leave floating
Power: Floating

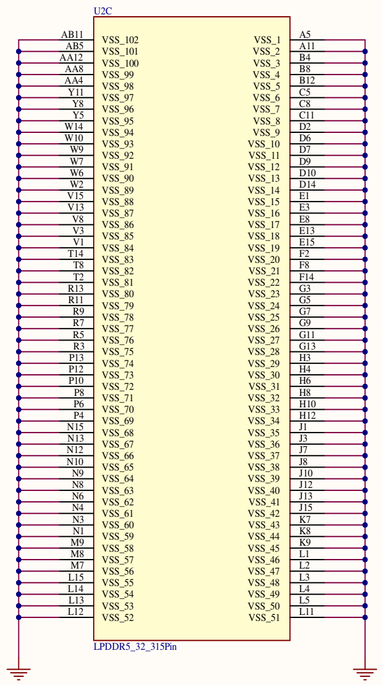
Title	*RK3588S_MIPI*		*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A2	Number: 36	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:45	Sheet 13 of 41	
File: RK3588S_MIPI.SchDoc		Designed by: neal.kim@hardkernel.com	

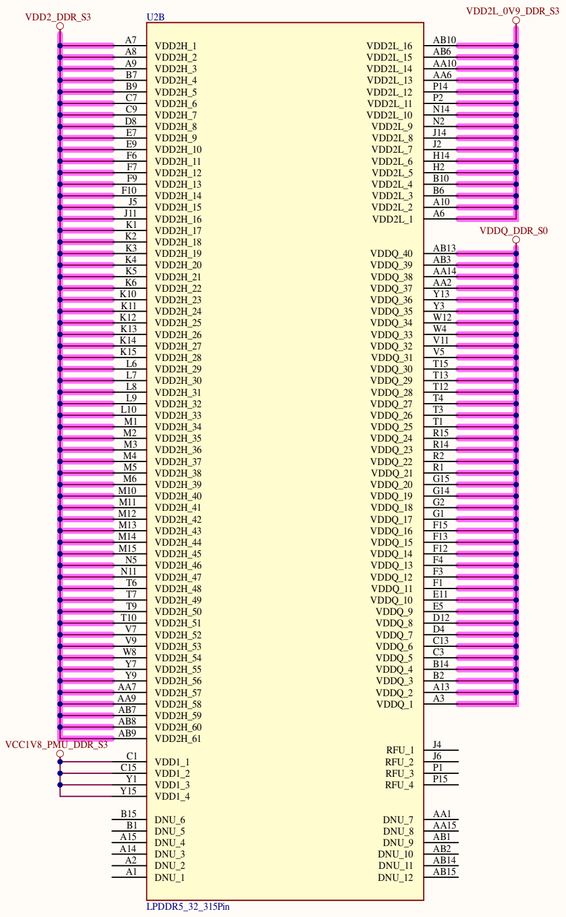
ODROID

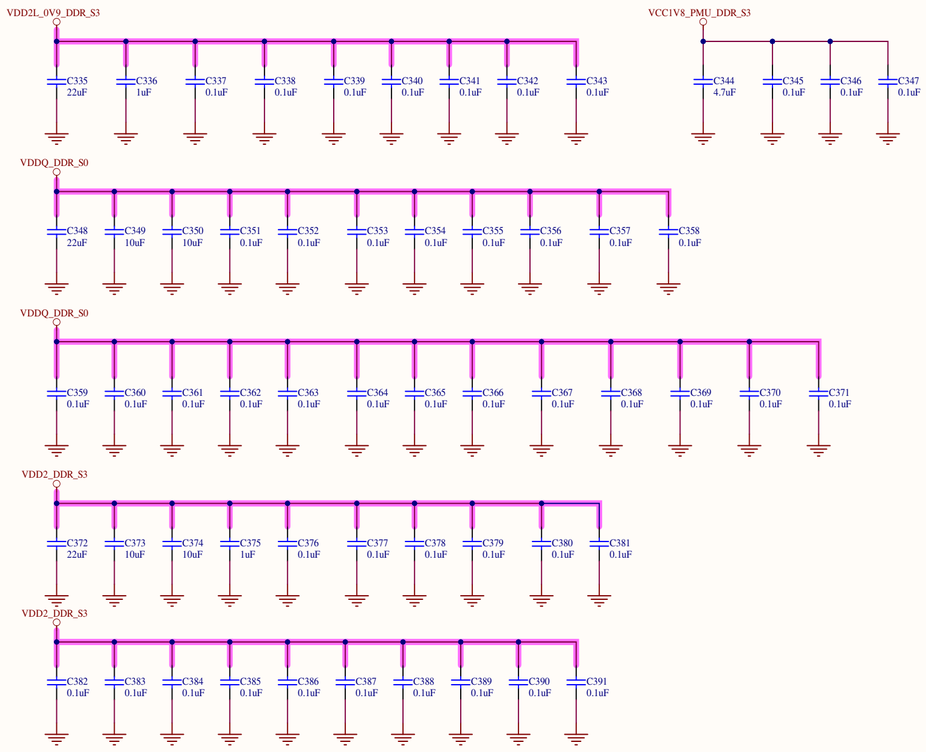
DRAM-LPDDR5_2X32bit



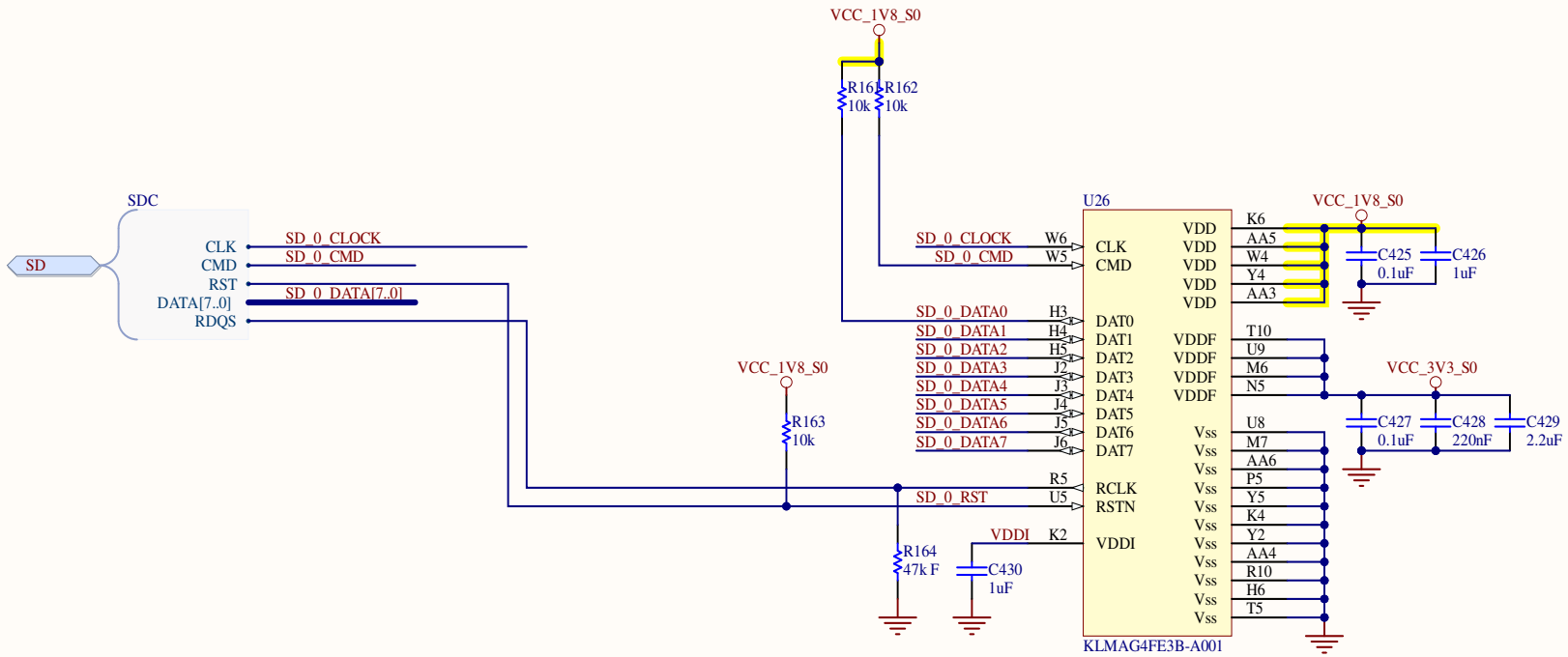








Title: DRAM-DDR4_2x16bit_200P			Hardkernel Co.,LTD. 475-1 Manamro Manangu, Anyang City Gyeonggido South Korea
Size: A2	Number: 4	Revision: 0.1	ODROID
Date: 2024-07-29	Time: 오후 4:15:45	Sheet 14 of 41	
File: DDR5_CH0_32bit_315PSchDoc		Designed by: neal.kim@hardkernel.com	

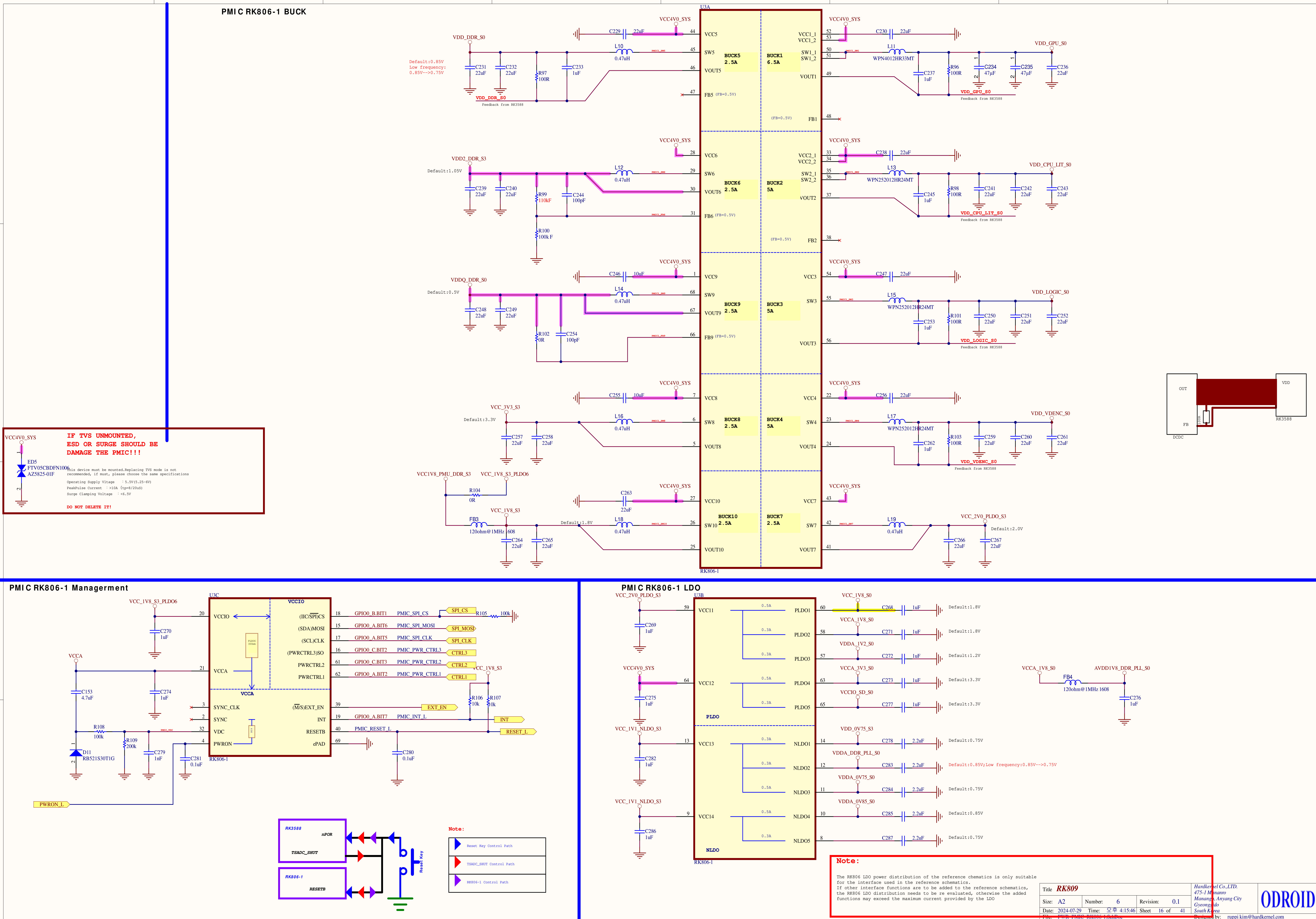


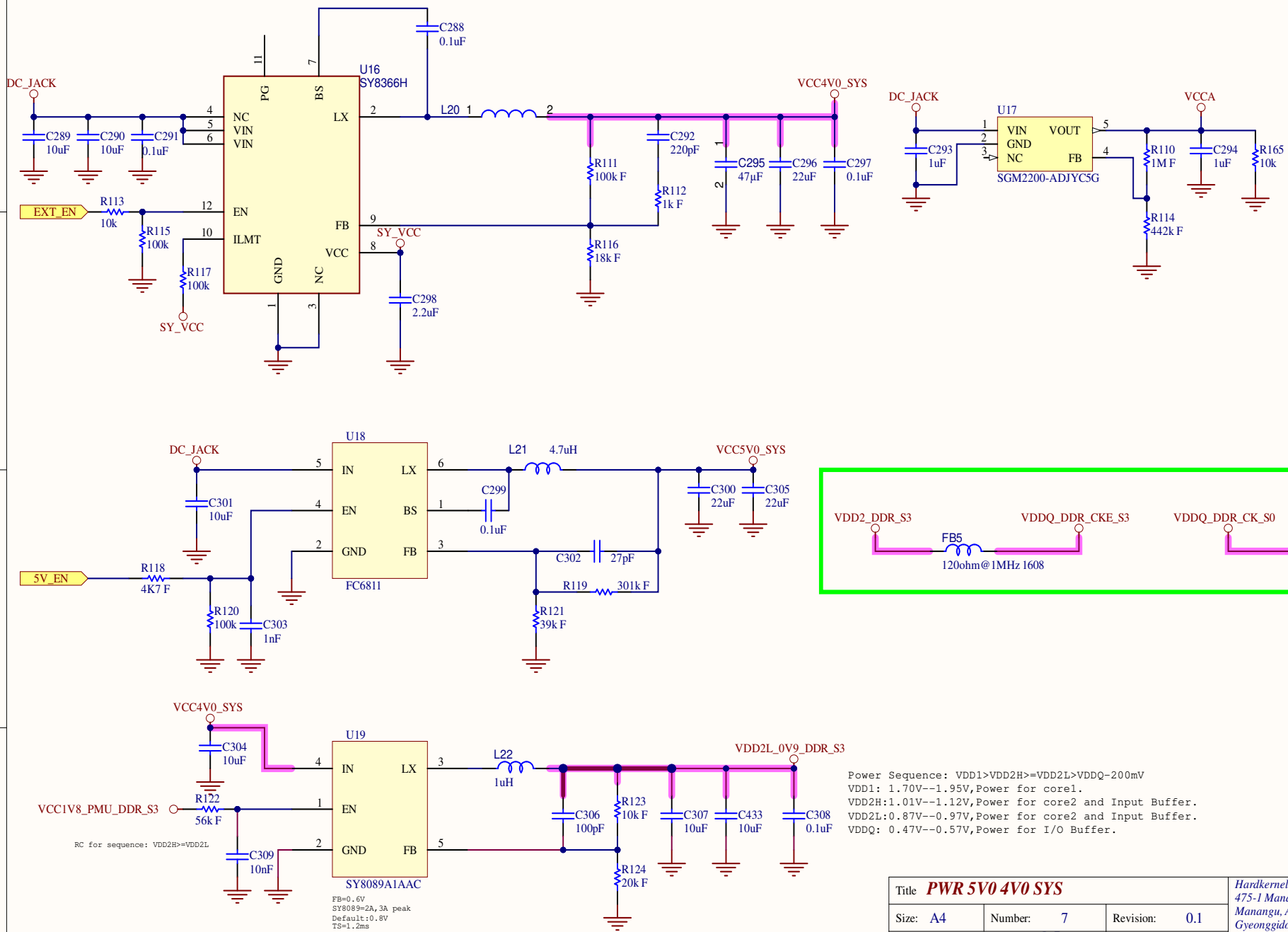
Title	**eMMC Connector**		
Size: A4	Number: 5	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 15 of 41	
File: EMMC.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

ODROID

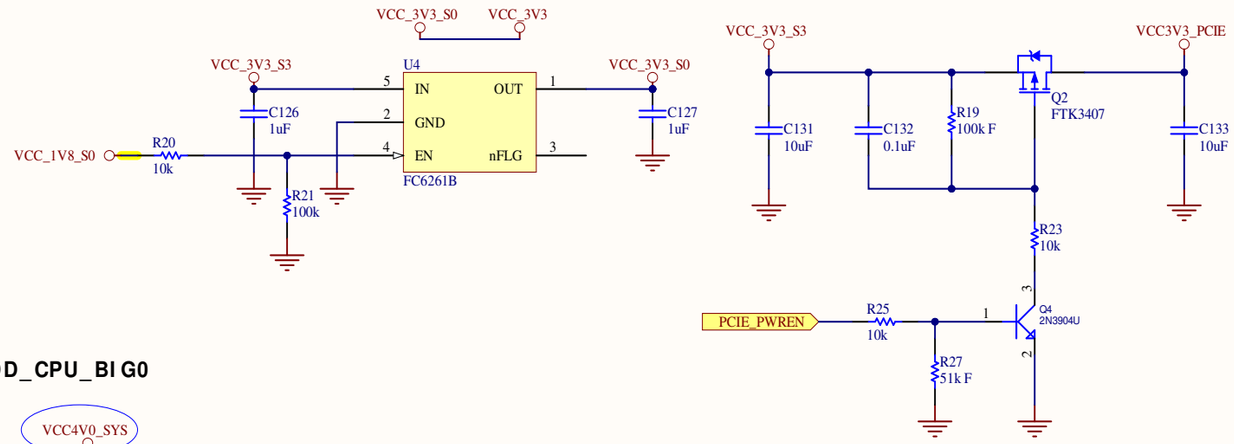

PMIC RK806-1 BUCK
U3A
VCC4V0_SYS
VDD_DDR_S0
Default:0.85V
Low frequency:
0.85V-->0.75V
C229 22uF
L10 0.47uH
C231 22uF
C232 22uF
R97 100R
C233 1uF
VDD_DDR_S0
Feedback from RK3588
VCC5
SW5
VOUT5
FB5 (FB=0.5V)
BUCK5 2.5A
BUCK1 6.5A
VCC1_1
VCC1_2
SW1_1
SW1_2
VOUT1
FB1
(FB=0.5V)
C230 22uF
L11 WPN4012H R33MT
VDD_GPU_S0
C237 1uF
R96 100R
C234 47uF
C235 47uF
C236 22uF
VDD_GPU_S0
Feedback from RK3588
VDD2_DDR_S3
Default:1.05V
L12 0.47uH
C239 22uF
C240 22uF
R99 110kF
C244 100pF
R100 100k F
VCC6
SW6
VOUT6
FB6 (FB=0.5V)
BUCK6 2.5A
BUCK2 5A
VCC2_1
VCC2_2
SW2_1
SW2_2
VOUT2
FB2
C238 22uF
L13 WPN252012H R24MT
VDD_CPU_LIT_S0
C245 1uF
R98 100R
C241 22uF
C242 22uF
C243 22uF
VDD_CPU_LIT_S0
Feedback from RK3588
VDDQ_DDR_S0
Default:0.5V
C246 10uF
L14 0.47uH
C248 22uF
C249 22uF
R102 0R
C254 100pF
VCC9
SW9
VOUT9
FB9 (FB=0.5V)
BUCK9 2.5A
BUCK3 5A
VCC3
SW3
VOUT3
C247 22uF
L15 WPN252012H R24MT
VDD_LOGIC_S0
C253 1uF
R101 100R
C250 22uF
C251 22uF
C252 22uF
VDD_LOGIC_S0
Feedback from RK3588
OUT
FB
DCDC
VDD
RK3588
VCC_3V3_S3
Default:3.3V
C255 10uF
L16 0.47uH
C257 22uF
C258 22uF
VCC8
SW8
VOUT8
BUCK8 2.5A
BUCK4 5A
VCC4
SW4
VOUT4
C256 22uF
L17 WPN252012H R24MT
VDD_VDENC_S0
C262 1uF
R103 100R
C259 22uF
C260 22uF
C261 22uF
VDD_VDENC_S0
Feedback from RK3588
VCC1V8_PMU_DDR_S3
VCC_1V8_S3_PLDO6
R104 0R
C263 22uF
VCC_1V8_S3
FB3 120ohm@1MHz 1608
Default:1.8V
L18 0.47uH
C264 22uF
C265 22uF
VCC10
SW10
VOUT10
BUCK10 2.5A
BUCK7 2.5A
VCC7
SW7
VOUT7
VCC_2V0_PLDO_S3
Default:2.0V
L19 0.47uH
C266 22uF
C267 22uF
RK806-1
VCC4V0_SYS
IF TVS UNMOUNTED,
ESD OR SURGE SHOULD BE
DAMAGE THE PMIC!!!
ED5
FTV05CBDFN1006
AZ5825-01F
this device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vitage : 5.5V(5.25-6V)
PeakPulse Current : >10A (tp=8/20uS)
Surge Clamping Voltage : <6.5V
DO NOT DELETE IT!
PMIC RK806-1 Management
U3C
VCC_1V8_S3_PLDO6
C270 1uF
VCCA
C153 4.7uF
C274 1uF
R108 100k
R109 200k
C279 1nF
C281 0.1uF
D11 RB521S30T1G
PWRON_L
VCCIO
VCCA
SYNC_CLK
SYNC
VDC
PWRON
(IIC/SPI)CS
(SDA)MOSI
(SCL)CLK
(PWRCTRL3)SO
PWRCTRL2
PWRCTRL1
(M/S)EXT_EN
INT
RESETB
ePAD
RK806-1
GPIO0_B.BIT1 PMIC_SPI_CS SPI_CS
GPIO0_A.BIT6 PMIC_SPI_MOSI SPI_MOSI
GPIO0_A.BIT5 PMIC_SPI_CLK SPI_CLK
GPIO0_C.BIT2 PMIC_PWR_CTRL3 CTRL3
GPIO0_C.BIT3 PMIC_PWR_CTRL2 CTRL2
GPIO0_A.BIT2 PMIC_PWR_CTRL1 CTRL1
R105 100k
VCC_1V8_S3
R106 10k
R107 10k
EXT_EN
GPIO0_A.BIT7 PMIC_INT_L INT
PMIC_RESET_L RESET_L
C280 0.1uF
RK3588
nPOR
TSADC_SHUT
RK806-1
RESETB
Reset Key
Note:
Reset Key Control Path
TSADC_SHUT Control Path
RK806-1 Control Path
PMIC RK806-1 LDO
U3B
VCC_2V0_PLDO_S3
C269 1uF
VCC11
VCC4V0_SYS
C275 1uF
VCC12
PLDO
VCC_1V1_NLDO_S3
C282 1uF
VCC13
VCC_1V1_NLDO_S3
C286 1uF
VCC14
NLDO
RK806-1
PLDO1 0.5A VCC_1V8_S0 C268 1uF Default:1.8V
PLDO2 0.3A VCCA_1V8_S0 C271 1uF Default:1.8V
PLDO3 0.3A VDDA_1V2_S0 C272 1uF Default:1.2V
PLDO4 0.5A VCCA_3V3_S0 C273 1uF Default:3.3V
PLDO5 0.3A VCCIO_SD_S0 C277 1uF Default:3.3V
NLDO1 0.3A VDD_0V75_S3 C278 2.2uF Default:0.75V
NLDO2 0.3A VDDA_DDR_PLL_S0 C283 2.2uF Default:0.85V;Low frequency:0.85V-->0.75V
NLDO3 0.5A VDDA_0V75_S0 C284 2.2uF Default:0.75V
NLDO4 0.5A VDDA_0V85_S0 C285 2.2uF Default:0.85V
NLDO5 0.3A C287 2.2uF Default:0.75V
VCCA_1V8_S0
FB4 120ohm@1MHz 1608
AVDD1V8_DDR_PLL_S0
C276 1uF
Note:
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO
Title RK809
Size: A2
Number: 6
Revision: 0.1
Date: 2024-07-29
Time: 오후 4:15:46
Sheet 16 of 41
File: PWR_PMIC_RK806-1.SchDoc
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: ruppi.kim@hardkernel.com
ODROID



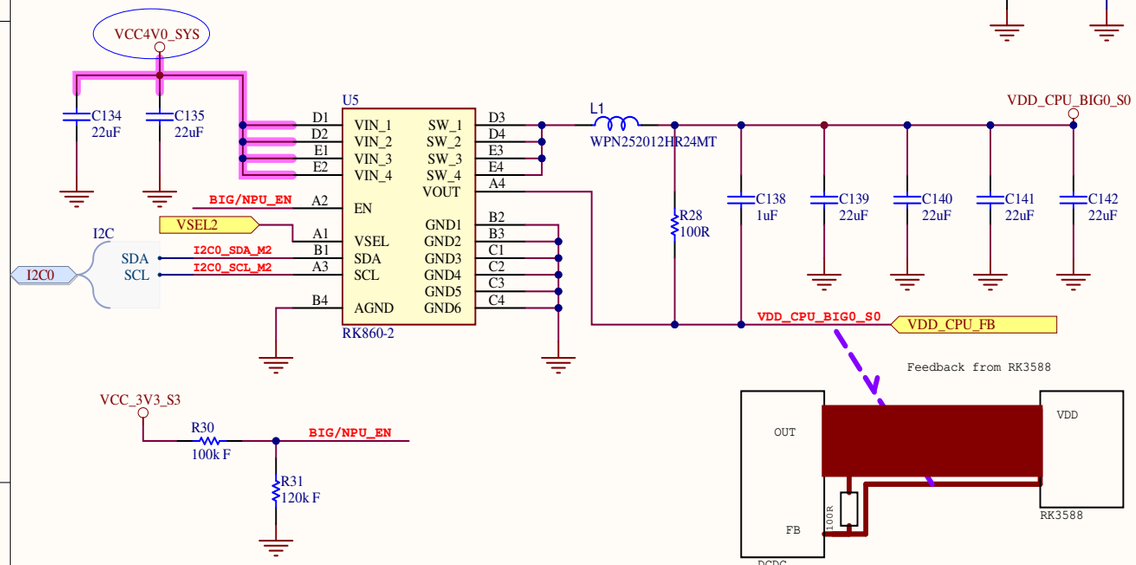
Title	PWR 5V0 4V0 SYS		
Size: A4	Number: 7	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 17 of 41	
File: PWR_5V0 4V0 SYS.SchDoc		Designed by: ruppi kim@hardkernel.com	

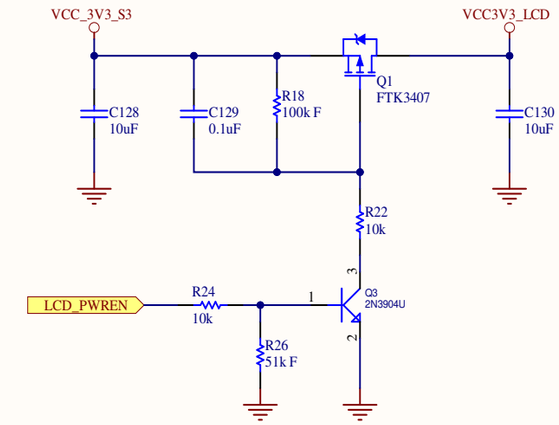
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

ODROID

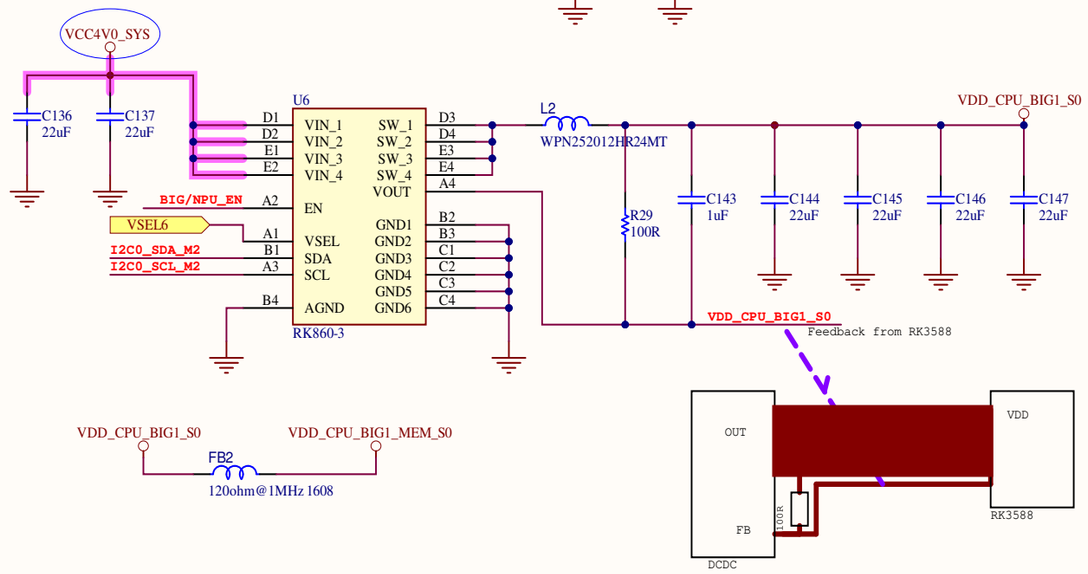


VDD_CPU_BIG0

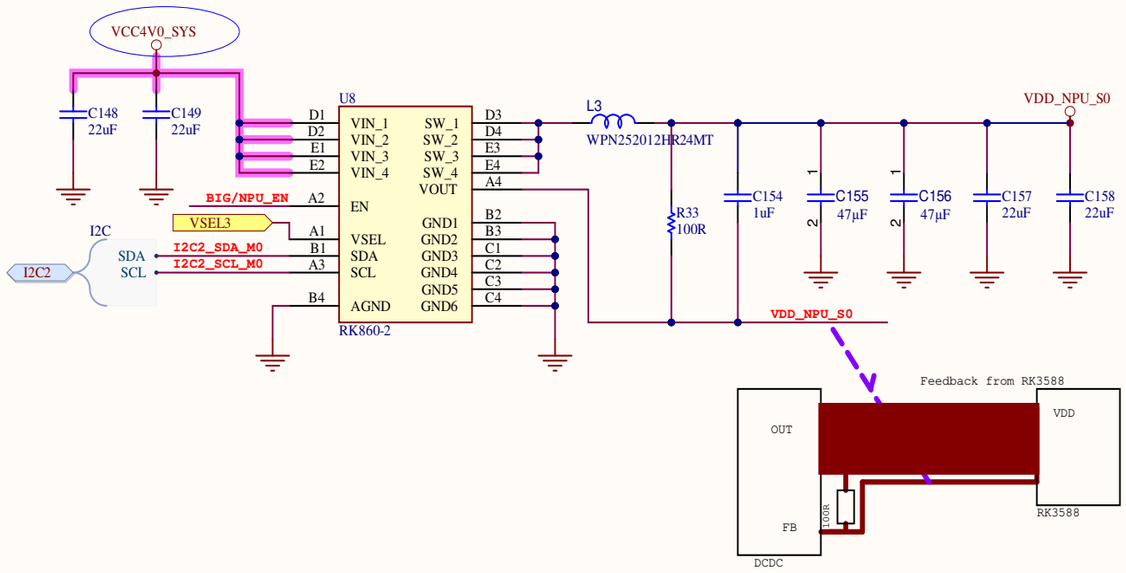


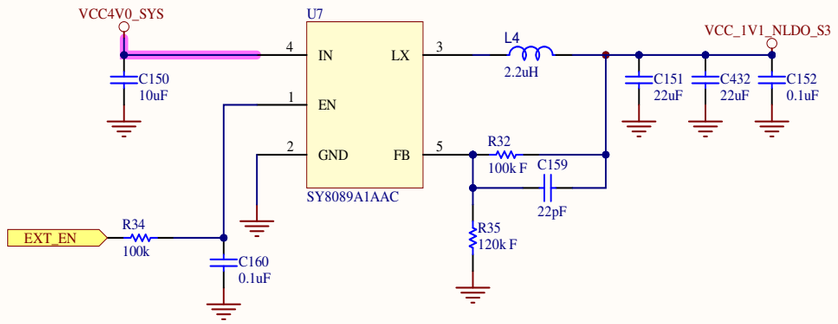


VDD_CPU_BIG1

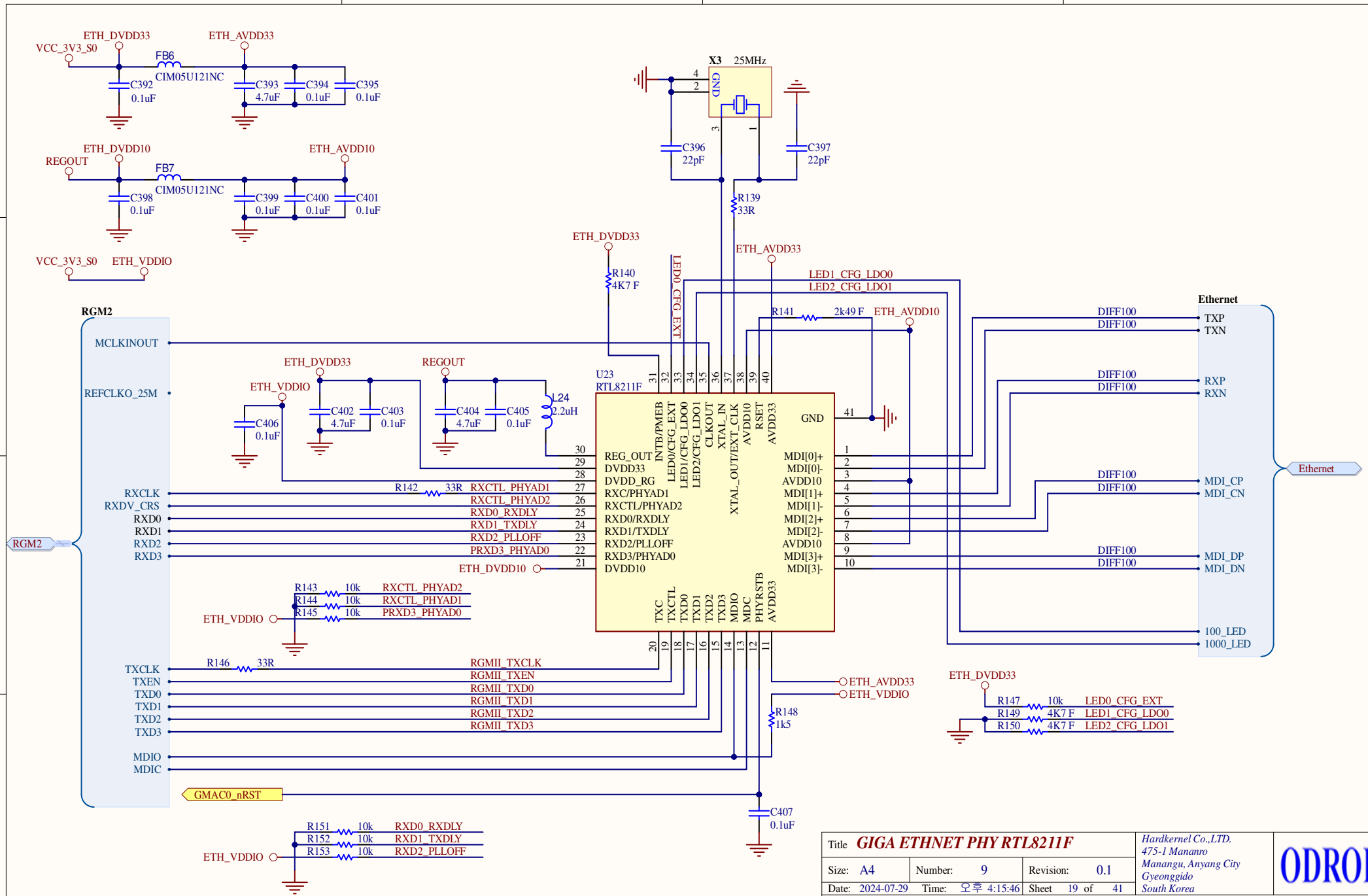


VDD_NPU





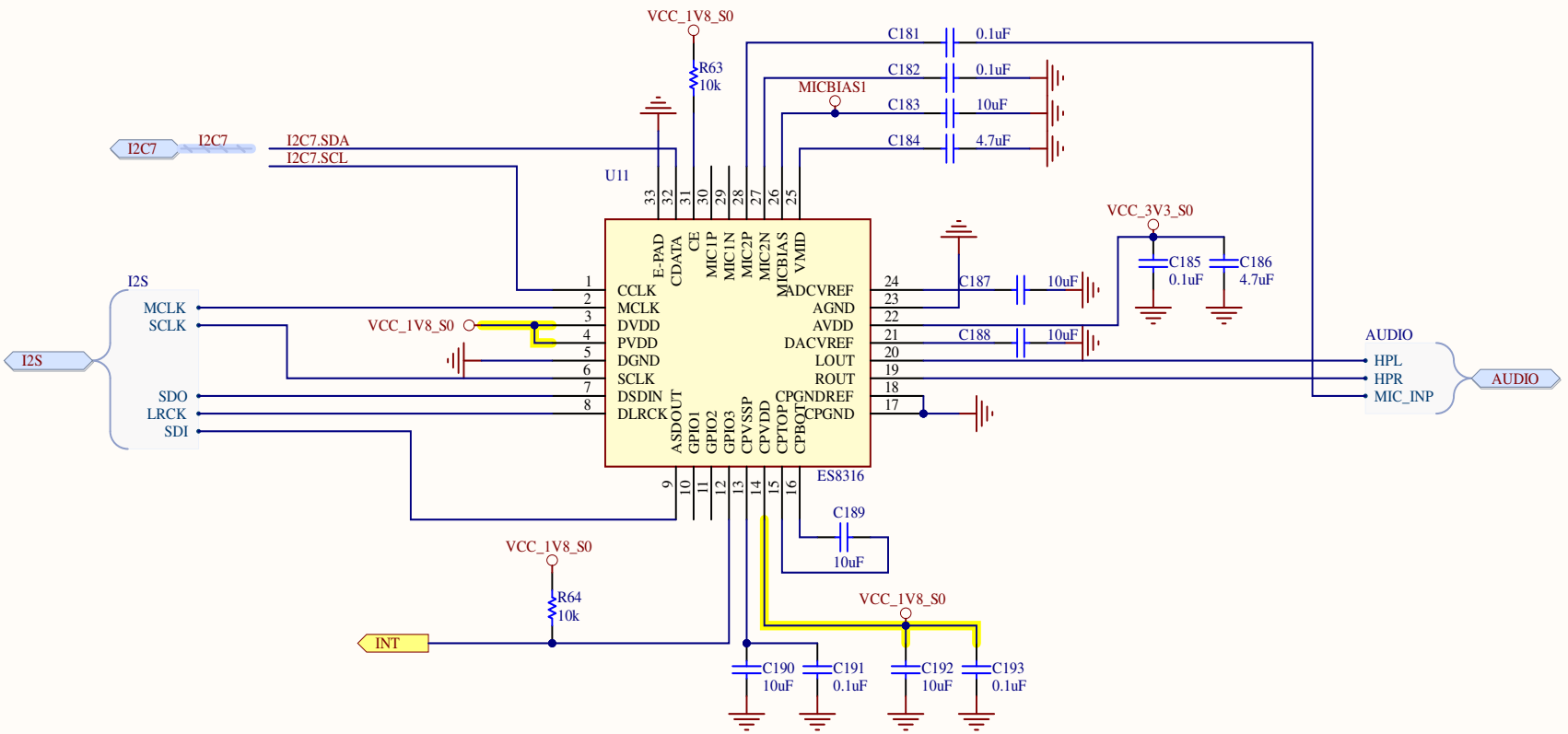
Title	PWR DCDC CPU GPU		Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea
Size: A3	Number: 8	Revision: 0.1	ODROID
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 18 of 41	
File: PWR_DCDC_CPU_GPU.SchDoc		Designed by: ruppi kim@hardkernel.com	



Title	GIGA ETHNET PHY RTL8211F		
Size: A4	Number: 9	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 19 of 41	
File: GIGA_ETHERNET_PHY_RT8211F.SchDoc		Designed by: ruppi.kim@hardkernel.com	

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

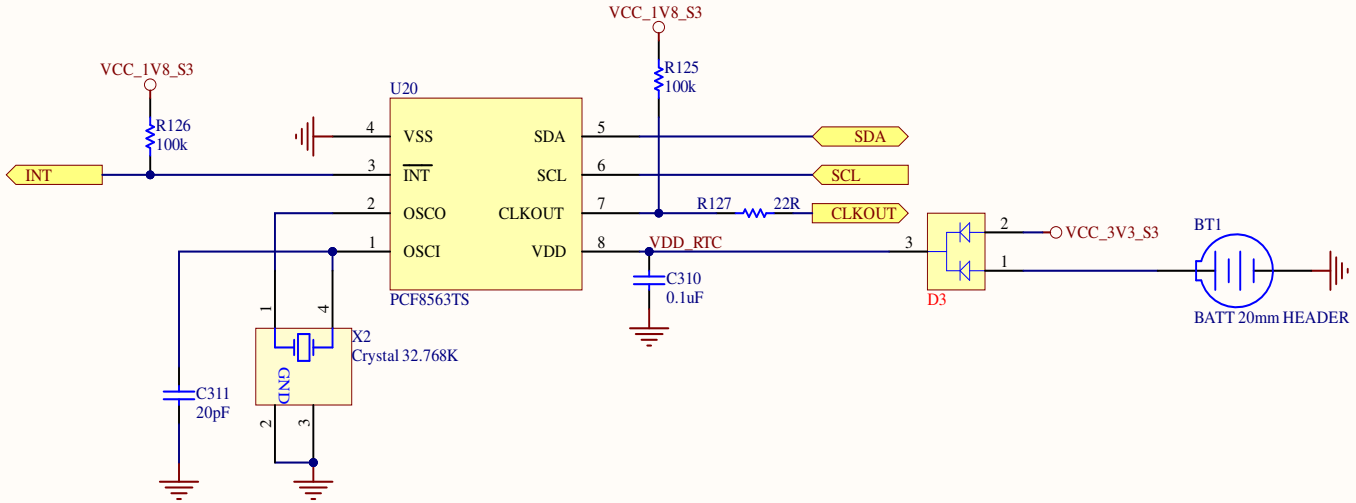
ODROID



Title	CODEC ES8316		
Size: A4	Number: 10	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 20 of 41	
File: CODEC_ES8316.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: *@hardkernel.com

ODROID

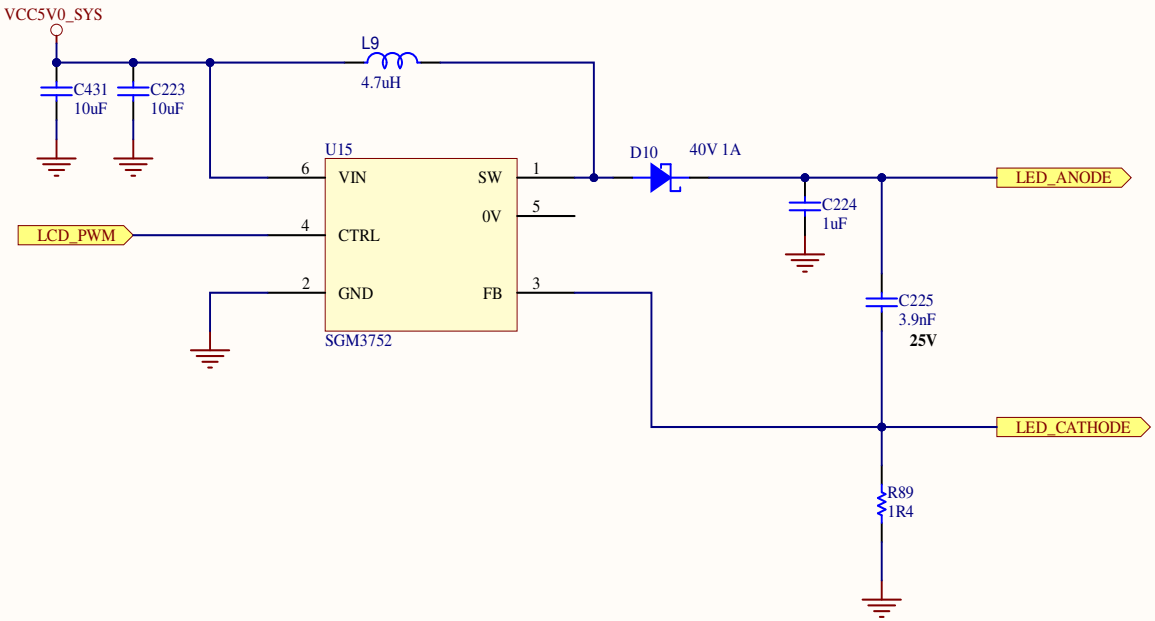


Title	**RTC PCF8563**		
Size: A4	Number: 11	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:46	Sheet 21 of 41	
File: RTC_PCF8663.SchDoc			

R&D PART
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: john lee

ODROID

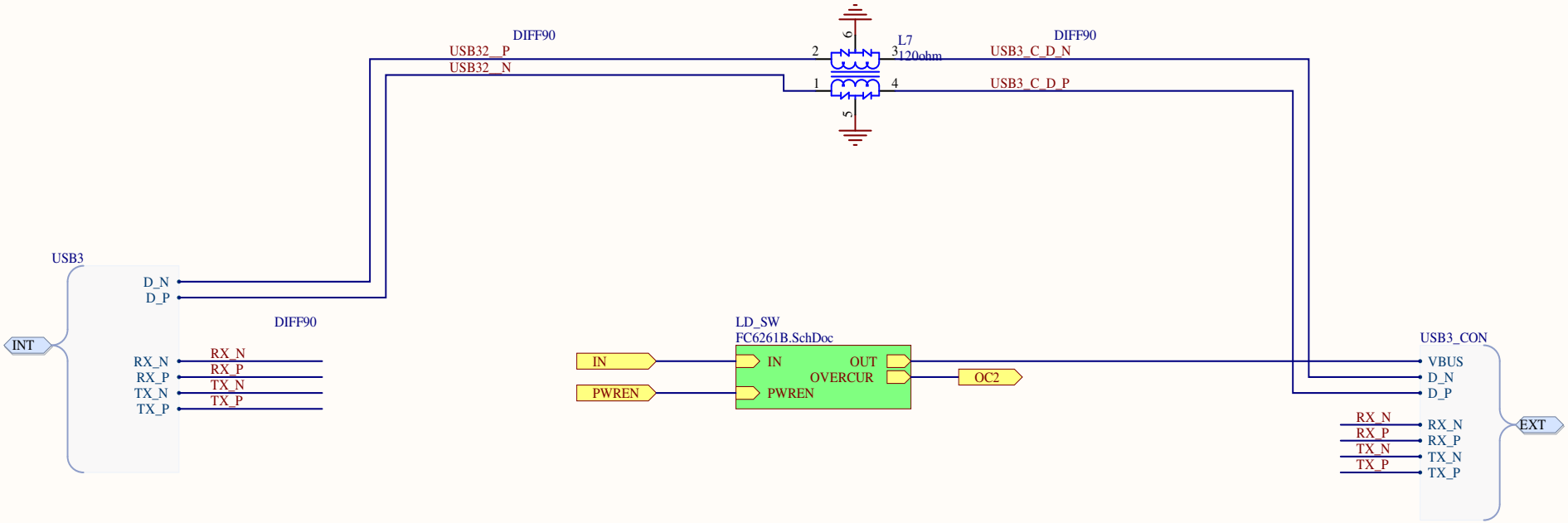


Title	**Backlight Driver**		
Size: A4	Number: 21	Revision:	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 22 of 41	
File: BACKLIGHT_SGM3752.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: neal.kim@hardkernel.com

ODROID

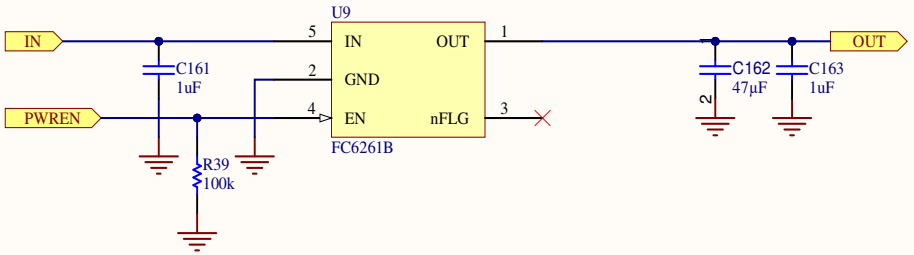


Title	**USB3 BUS POWER**		
Size: A4	Number: 22	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 23 of 41	
File: USB3_BUS_PWR.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

ODROID

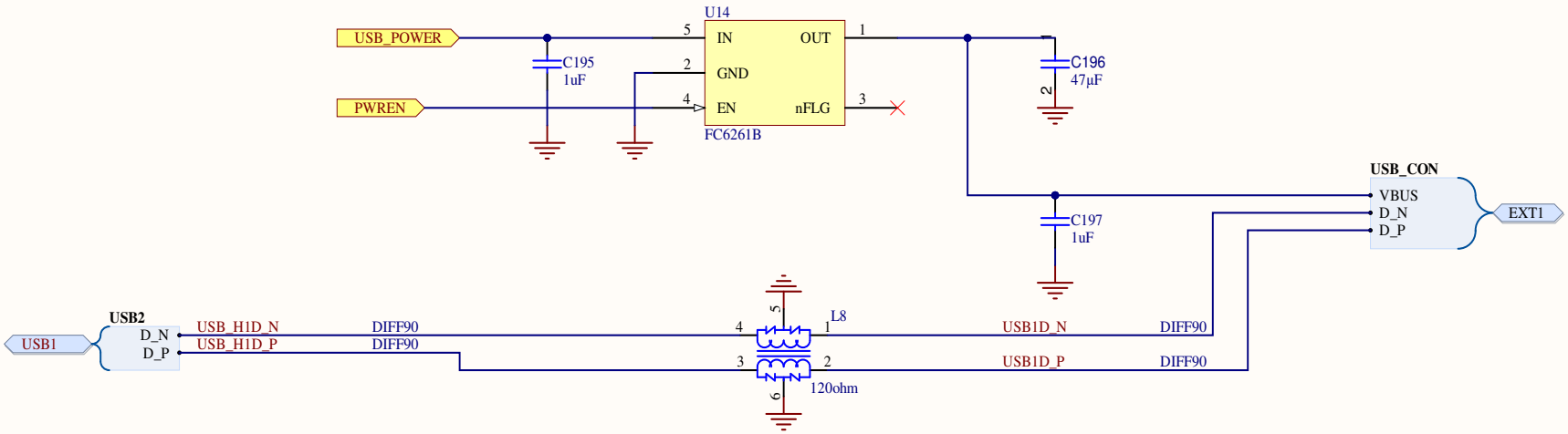


Title	**USB HOST Power Switch**		
Size: A4	Number: 25	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 24 of 41	
File: FC6261B.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

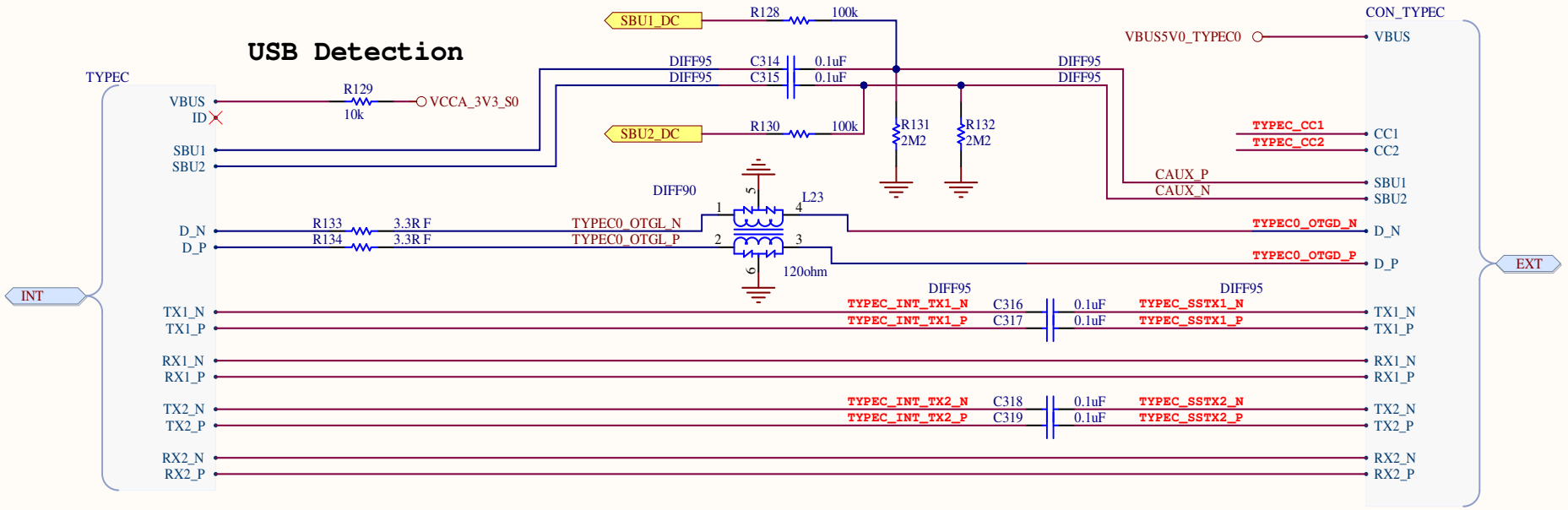
ODROID

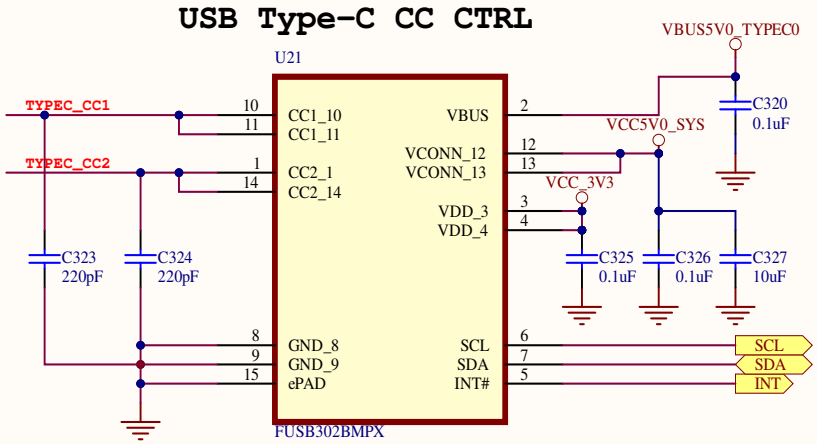


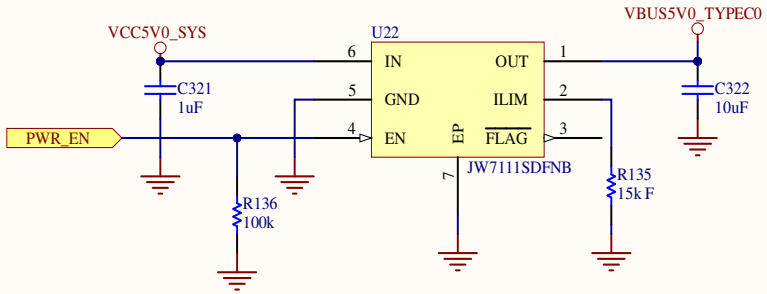
Title	USB HOST PWR SW		
Size: A4	Number: 23	Revision: 0.3	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 25 of 41	
File: USB_HOST_PWR_SW.SchDoc			

Hardkernel Co.,LTD.
1-605 Shinan Metrokhan 1115
Dalandong, Dongangu, Anyang
Gyeonggido
South Korea
Designed by: ruppi.kim@hardkernel.com

ODROID



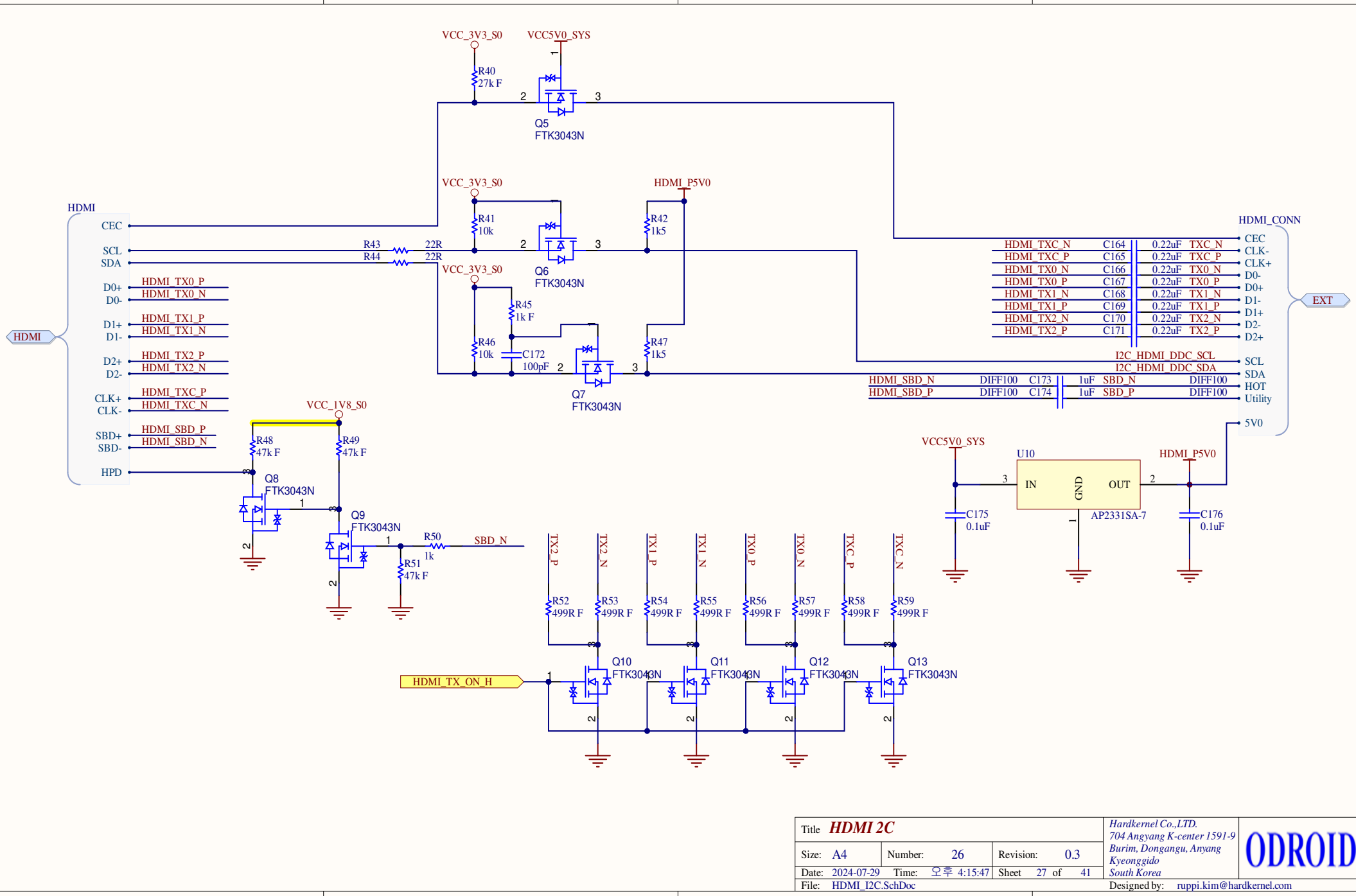




Title	*USB3.0 Type-C Connector*		
Size: A4	Number: 24	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 26 of 41	
File: USB3.0_TYPEC.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: ruppi.kim@hardkernel.com

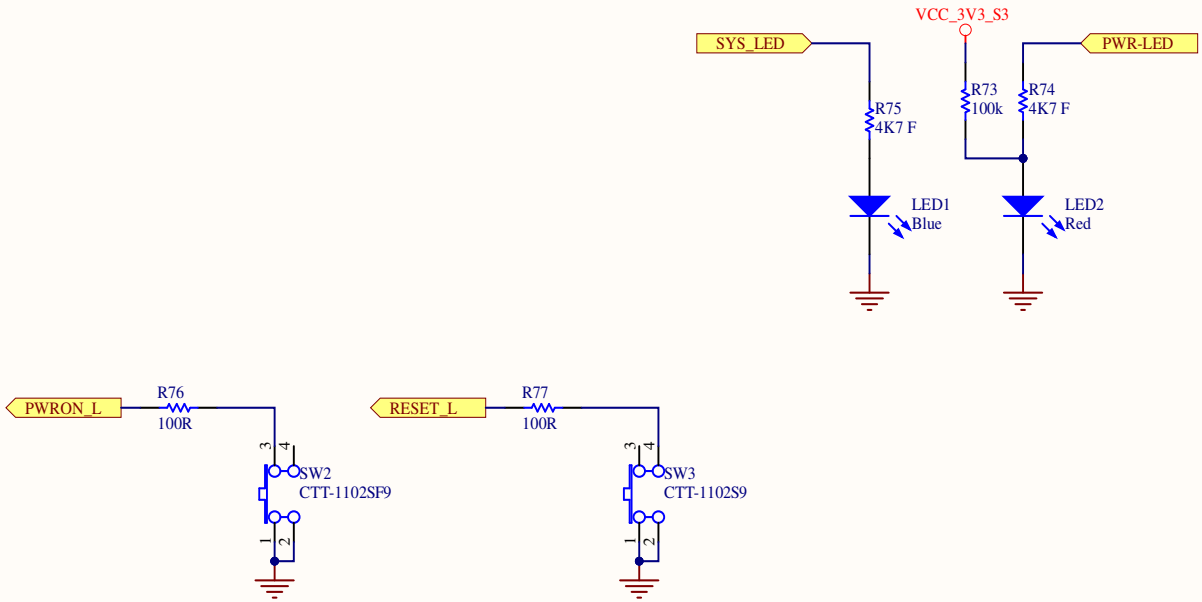
ODROID



Title	HDMI 2C		
Size: A4	Number: 26	Revision: 0.3	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 27 of 41	
File: HDMI_I2C.SchDoc			

Hardkernel Co.,LTD.
704 Angyang K-center 1591-9
Burim, Dongangu, Anyang
Kyeonggido
South Korea
Designed by: ruppi.kim@hardkernel.com

ODROID

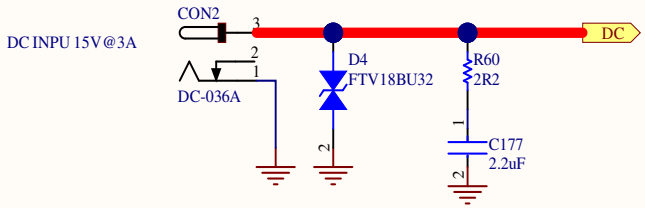


Title	***Indicator LEDs***		
Size: A4	Number: 27	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 28 of 41	
File: M2_LEDS.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

ODROID

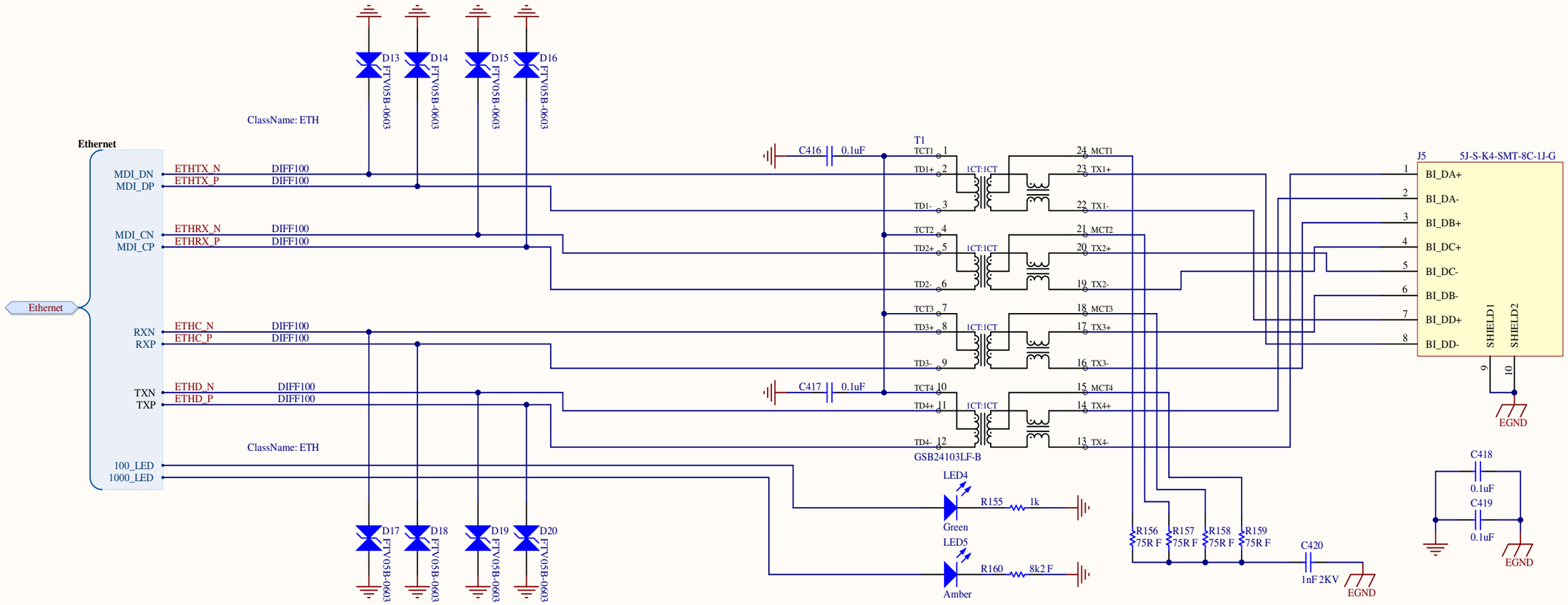


Title	**DC Jack**		
Size: A4	Number: 28	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 29 of 41	
File: CON_DCJACK.SchDoc			

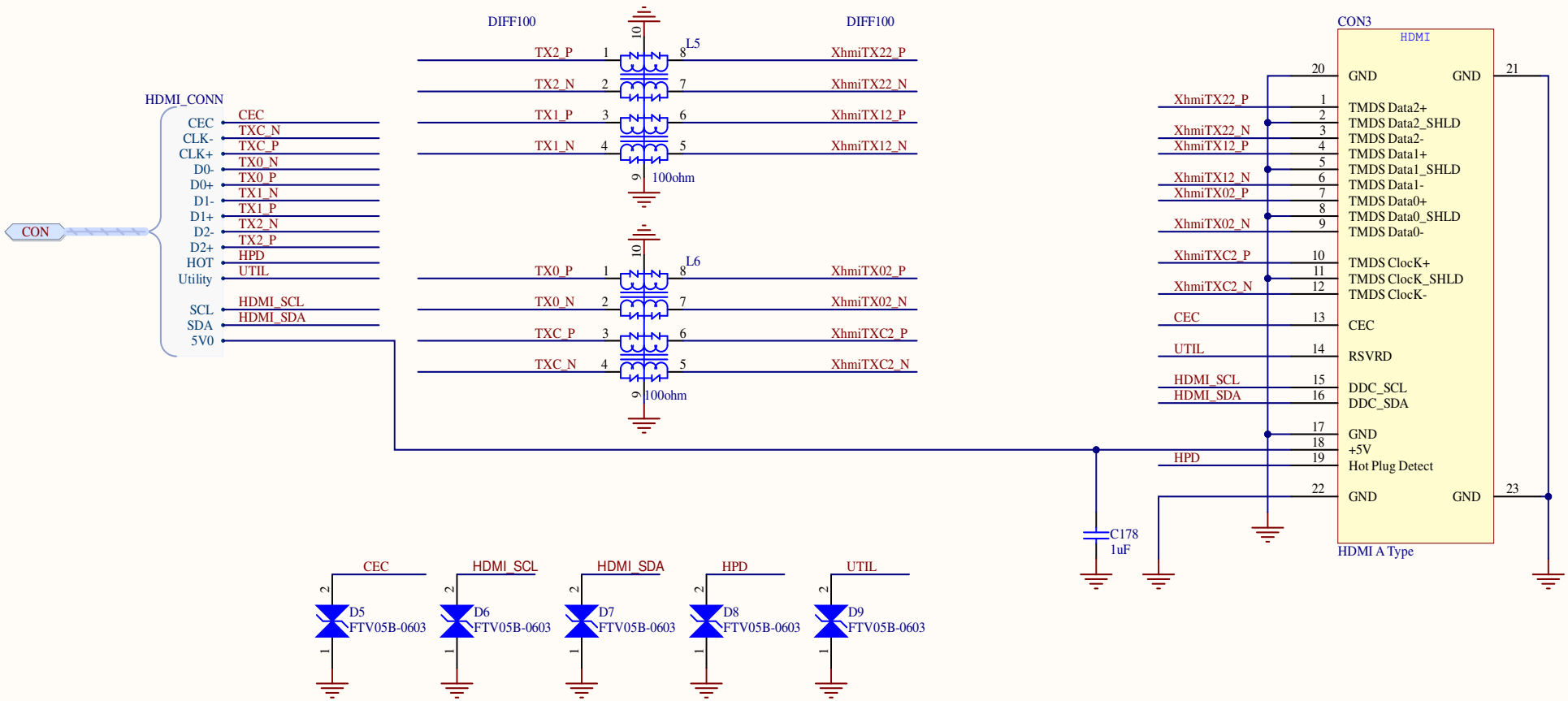
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

ODROID



Title	*Giga Ethernet Connector*		*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A3	Number: 29	Revision: 0.1	ODROID
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 30 of 41	
File: CON_GIGA_ETH.SchDoc		Designed by: ruppi.kim@hardkernel.com	

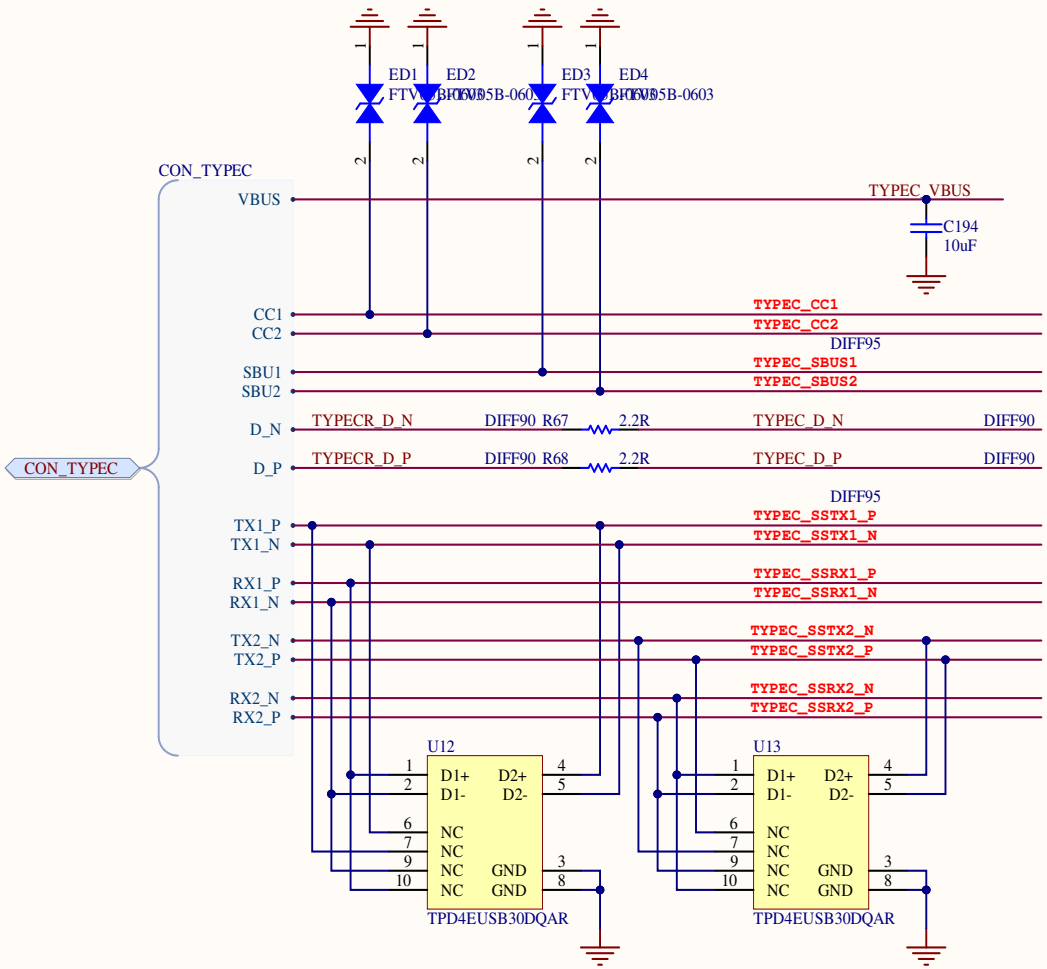


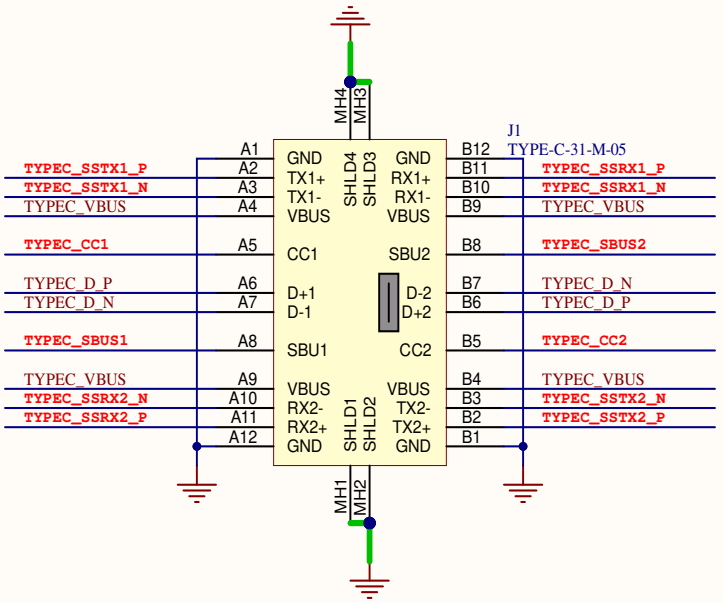
Title	**HDMI Type A Connector**		
Size: A4	Number: 30	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 31 of 41	
File: CON_HDMI.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi.kim@hardkernel.com

ODROID



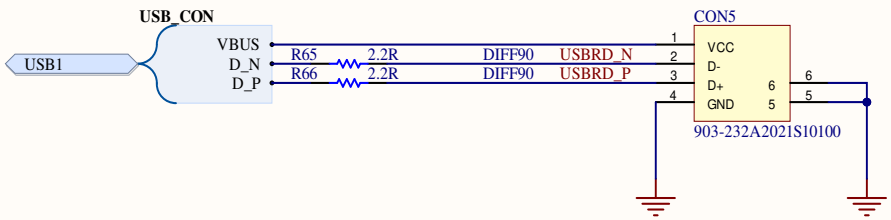


Title	*USB 3.0 Type C Connector*		
Size: A4	Number: 31	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 32 of 41	
File: CON_USB3.0_TYPEC.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

ODROID

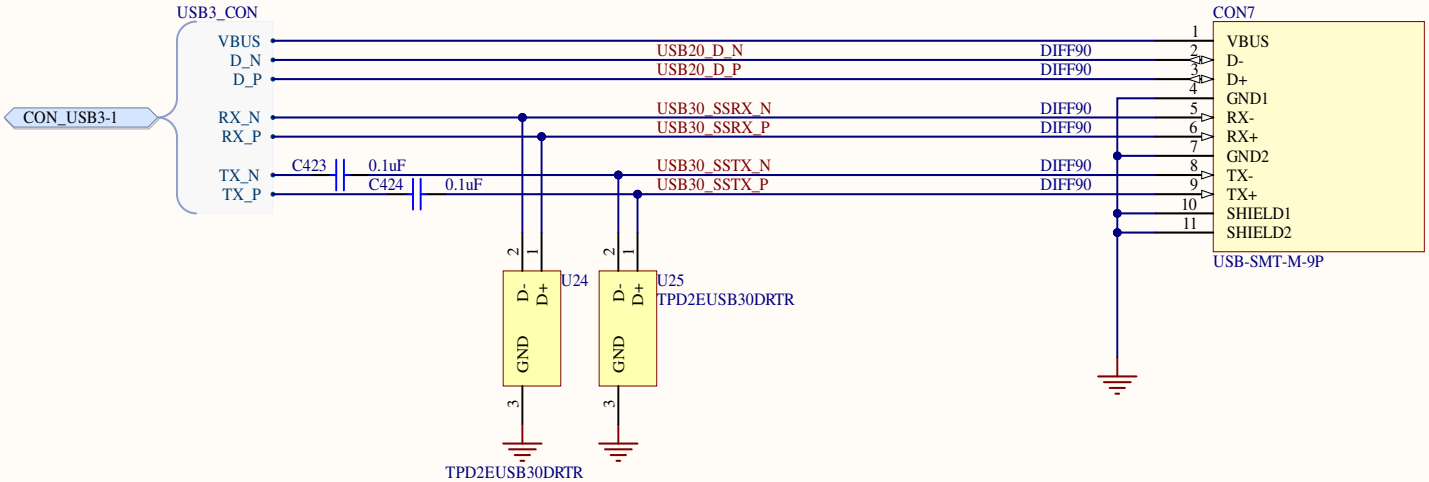


Title	*USB 2.0 Type A Connector*		
Size: A4	Number: 32	Revision: 0.3	
Date: 2024-07-29	Time: 오후 4:15:47	Sheet 33 of 41	
File: CON_USB_RA.SchDoc			

Hardkernel Co.,LTD.
1-605 Shinan Metrokhan 1115
Dalandong, Dongangu, Anyang
Gyeonggido
South Korea

Designed by: ruppi.kim@hardkernel.com

ODROID

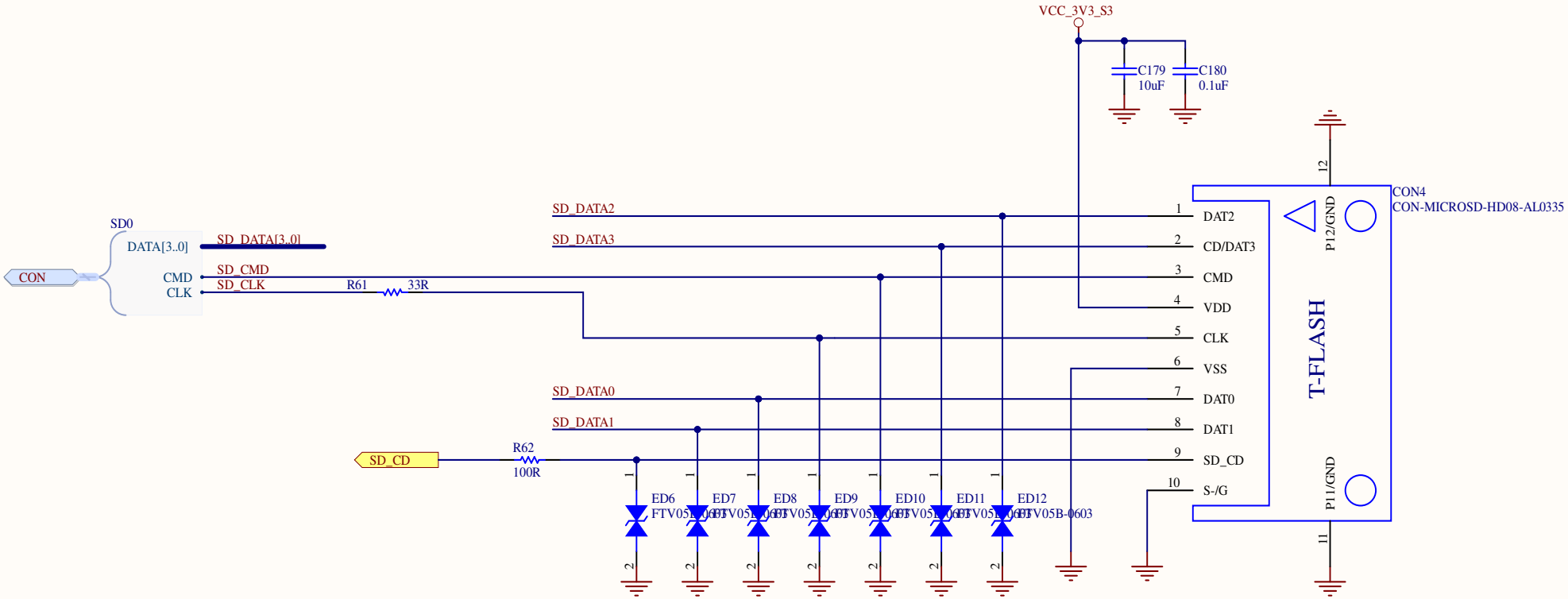


Title	*USB 3.0 Type A Connector*		
Size: A4	Number: 33	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 34 of 41	
File: CON_USB3_RA.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

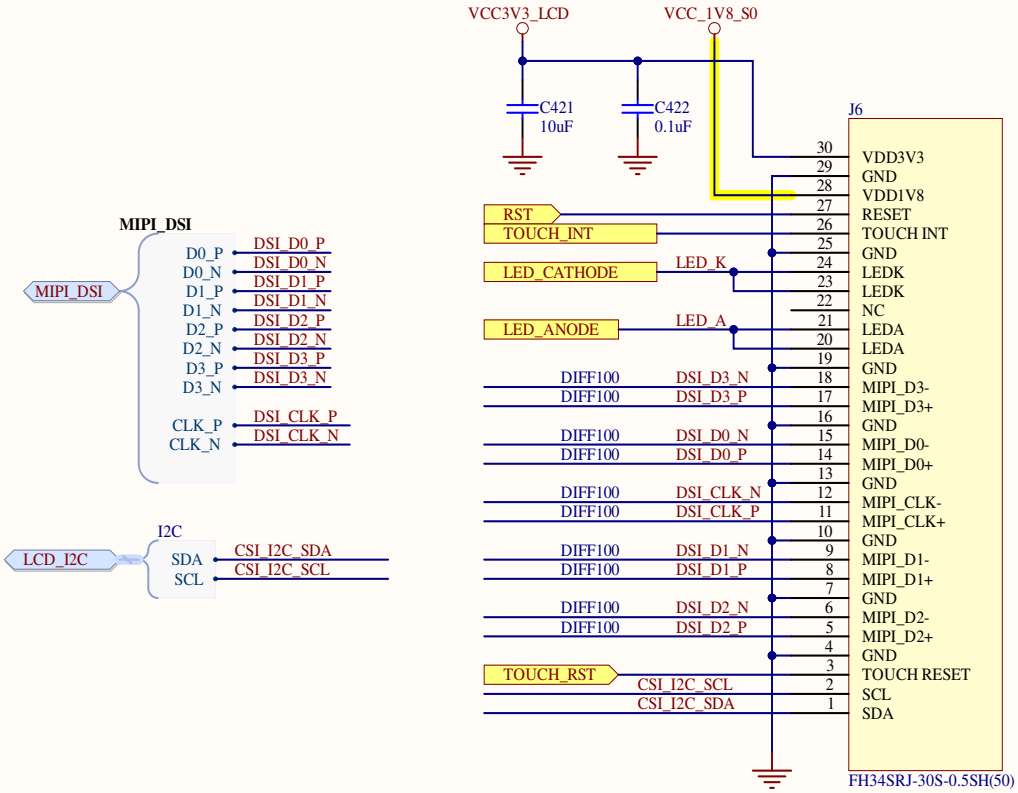
ODROID



Title	*Micro SD Socket*		
Size: A4	Number: 34	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 35 of 41	
File: CON_MICROSD_HD08-AL00335.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: ruppi kim@hardkernel.com

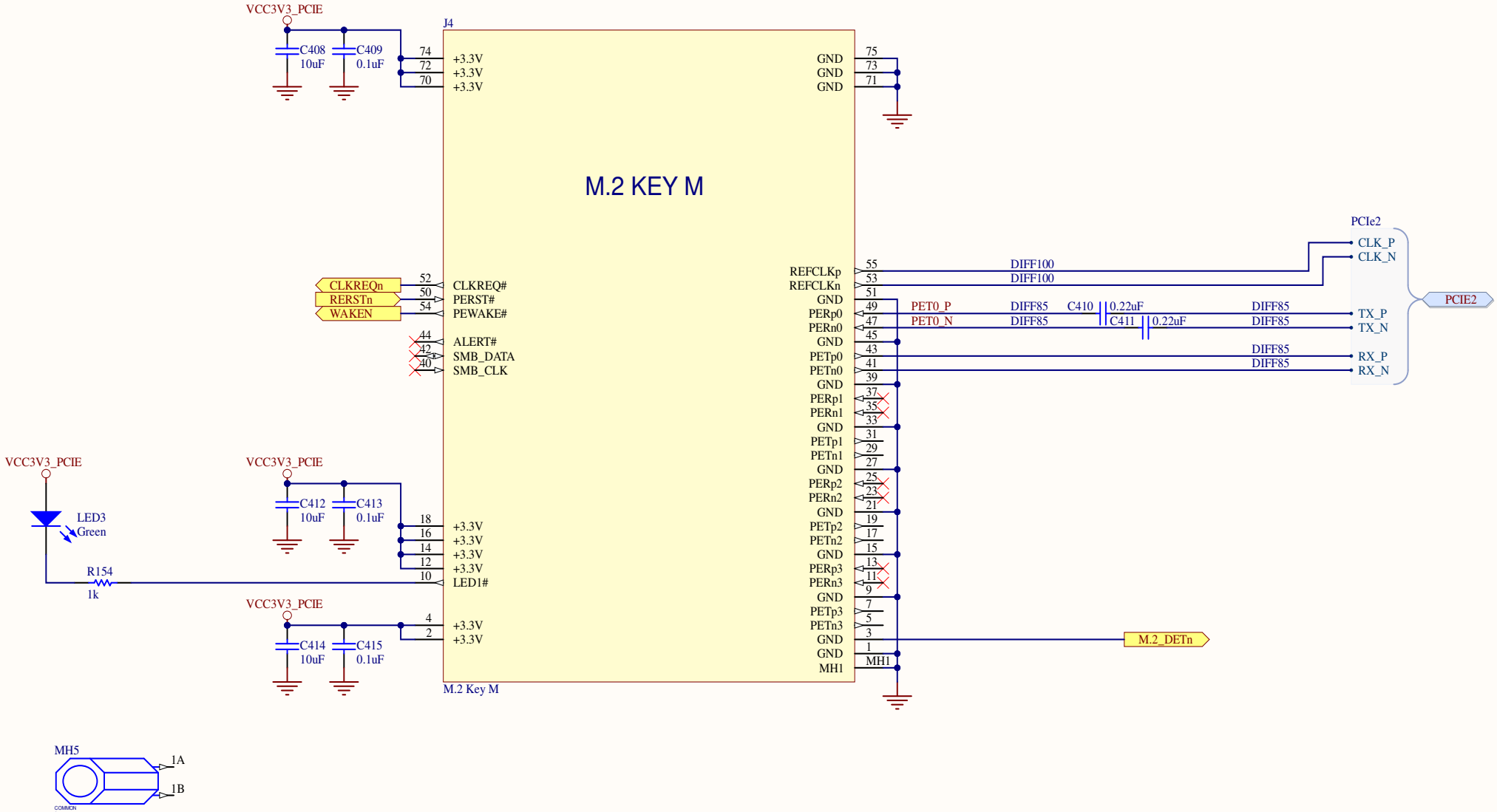
ODROID



Title	*CON LCD KD50T048-A*		
Size: A4	Number: 35	Revision: 1.0	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 36 of 41	
File: CON_LCD_FH34SRJ-30S_MIPI.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: *@hardkernel.com

ODROID

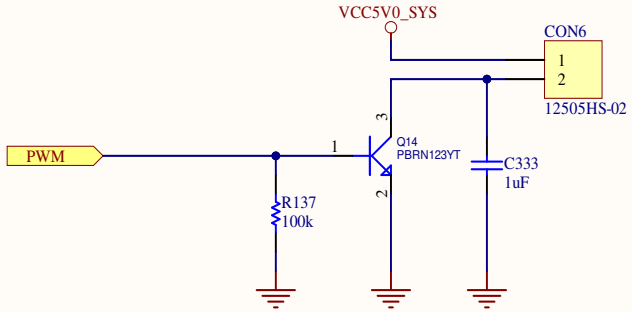


Title	***M.2 KEY M Connector***		
Size: A4	Number: 37	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 37 of 41	
File: CON_M2.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi kim@hardkernel.com

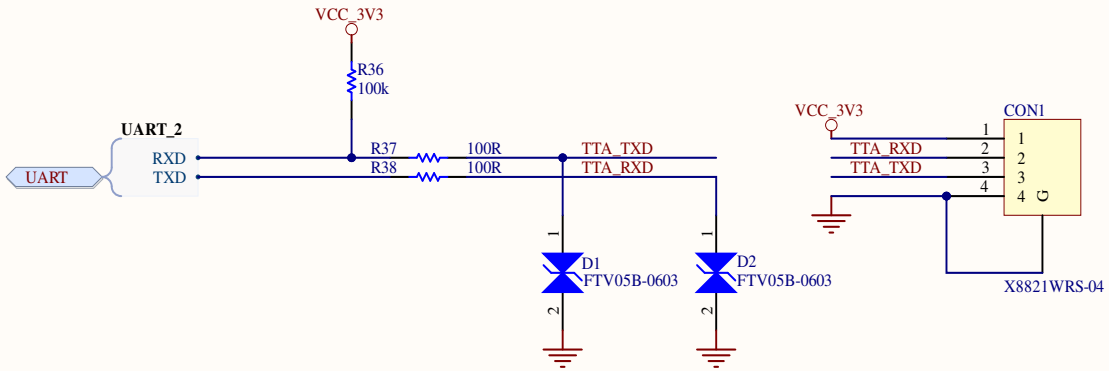
ODROID



Title	***FAN Connector***		
Size: A4	Number: 38	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 38 of 41	
File: CON_FAN.SchDoc			

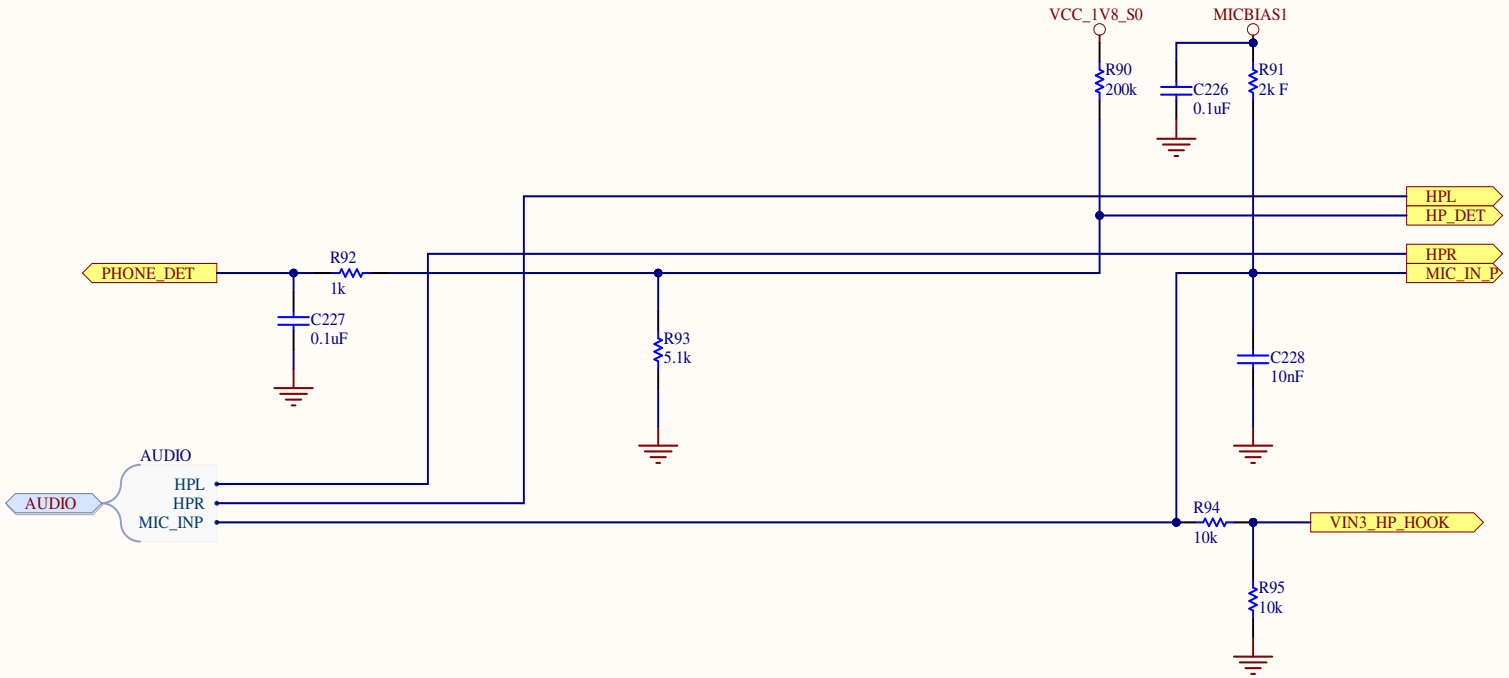
Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea
Designed by: *@hardkernel.com

ODROID



Title: *UART Connector*			*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A4	Number: 39	Revision: 0.1	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 39 of 41	
File: CON_UART.SchDoc		Designed by: ruppi.kim@hardkernel.com	

ODROID



Title	*Audio*		
Size: A4	Number: 40	Revision: 0.3	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 40 of 41	
File: CON_AUDIO.SchDoc			

Hardkernel Co.,LTD.
475-1 Mananro
Manangu, Anyang City
Gyeonggido
South Korea

Designed by: ruppi.kim@hardkernel.com

ODROID

HW REVISION	DATE	Change Note
v1.0	2024.01.24	1. The Sample First revision.
v1.0	2024.03.10	1. Power of MicroSD changed to VCC_3V3_S3 2. Swap 11 and 13 pin of J2 3. Swap SPI MOSI and SPI CLK for the RK806-1 4. Fixed incorrectly connected HDMI signals 5. Switch positions 1 and 3 of the SLIDE SW Footprint(Boot Mode) 6. Pin# 28 of J6 connect to VCC_1V8_S0 7. Modify GPIOs of expansion Port 8. Add two test points for MASKROM boot mode 9. Remove D3 and connected to HDMI_5V0 10. Swap TYPECD_N and D_P the Type C USB connector's B6, B7 11. Replace SY8080A1AAC U19 and U7. 12. Pin# 38 of J2 connect to VCC_1V8_S0 13. Add one-shot circuit for VDC of PMIC
v1.0	2024.06.11	1. The first mass production revision.

Title	***Revision History***		*Hardkernel Co.,LTD.* *475-1 Mananro* *Manangu, Anyang City* *Gyeonggido* *South Korea*
Size: A3	Number: 41	Revision:	
Date: 2024-07-29	Time: 오후 4:15:48	Sheet 41 of 41	
File: M2_REV_HISTORY.SchDoc		Designed by: neal.kim@hardkernel.com	