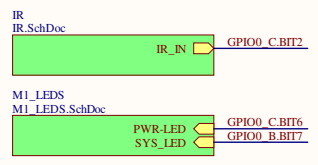
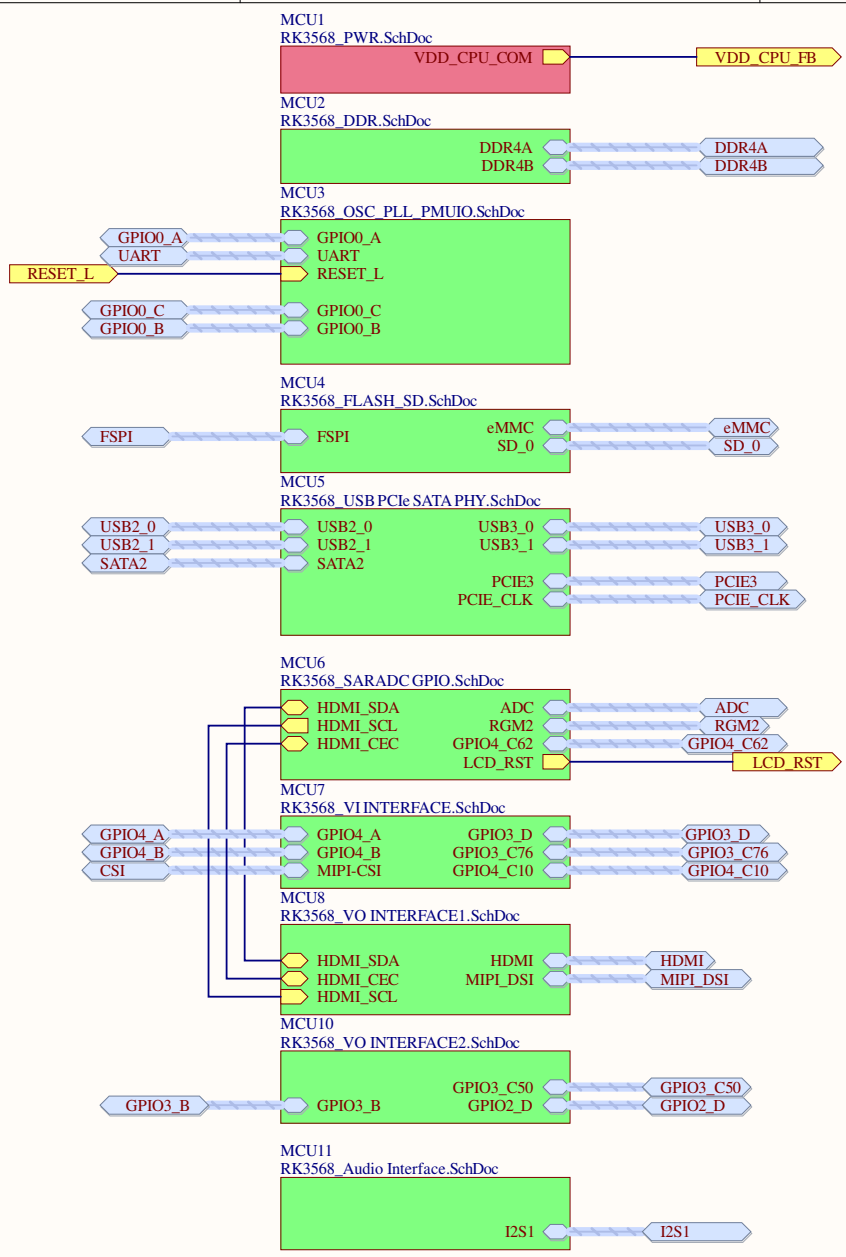


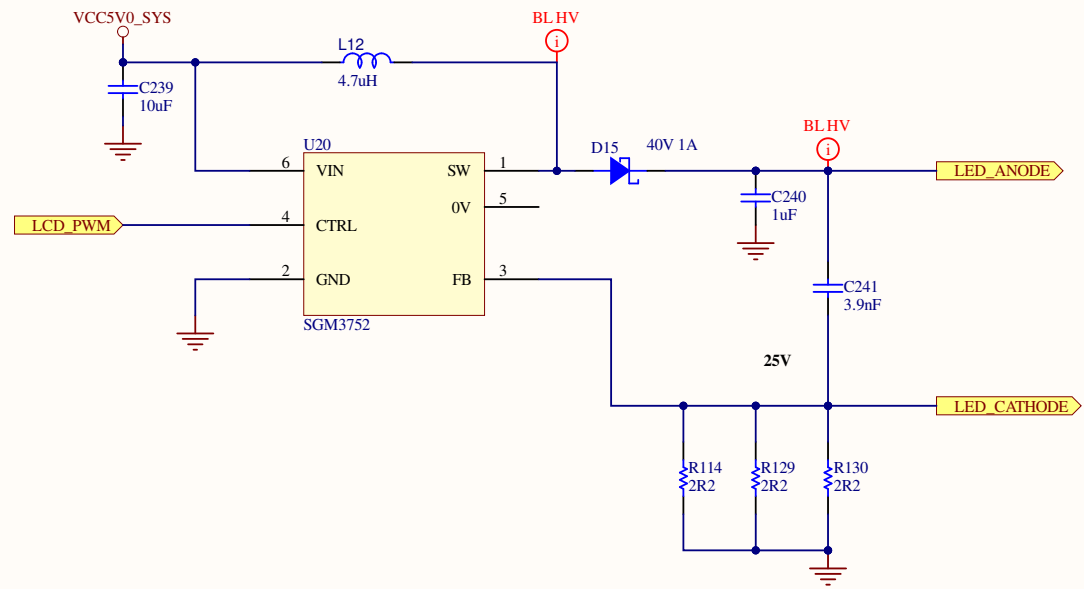
Mounting Holes



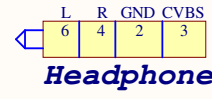
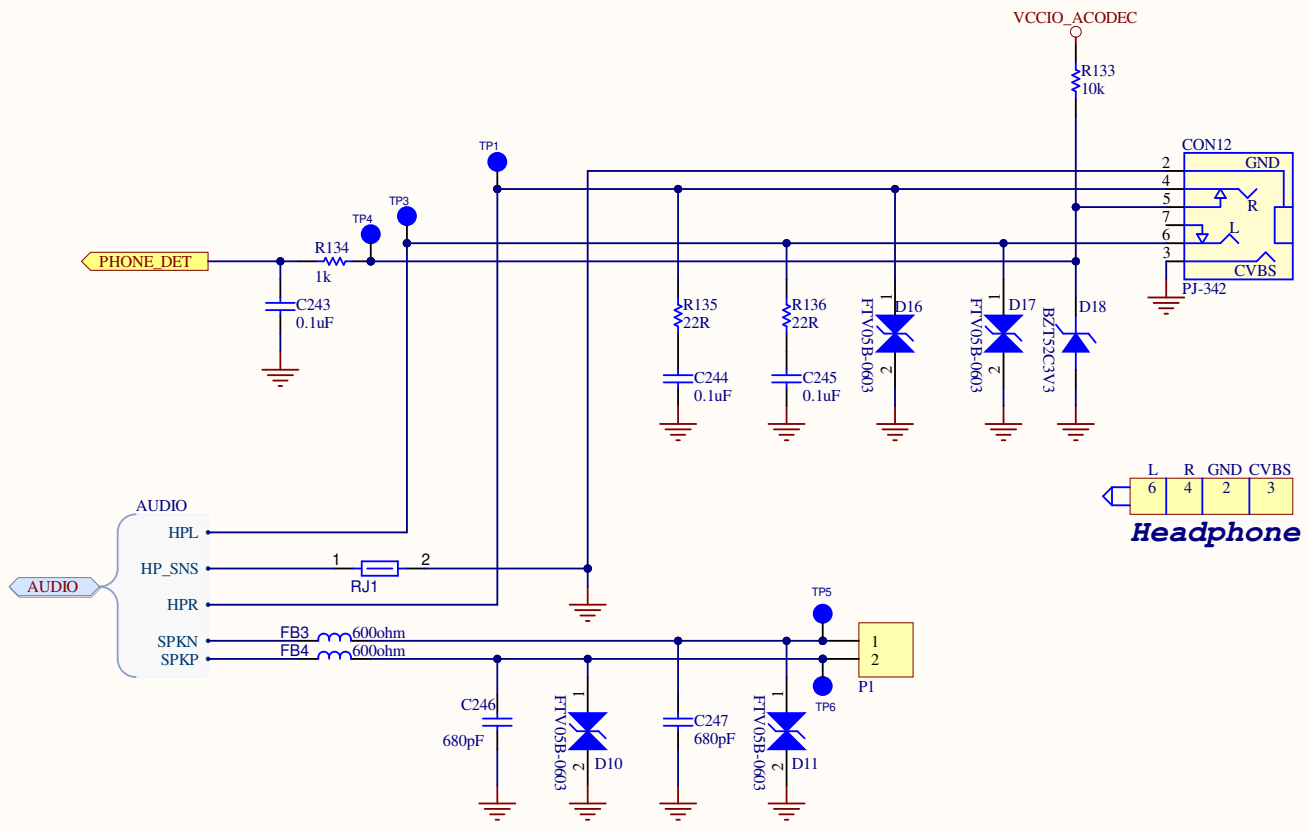
Title M1-MAIN		475-1 Mainano		Hardkernel Co., LTD.	
Size: A3	Number: 1.	Revision: 0.1	Manangu, Anyang City		ODROID
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 1 of 42	Gyeongdo		
File: M1-MAIN.SchDoc			South Korea		
			Designed by: ruppi.kim@hardkernel.com		



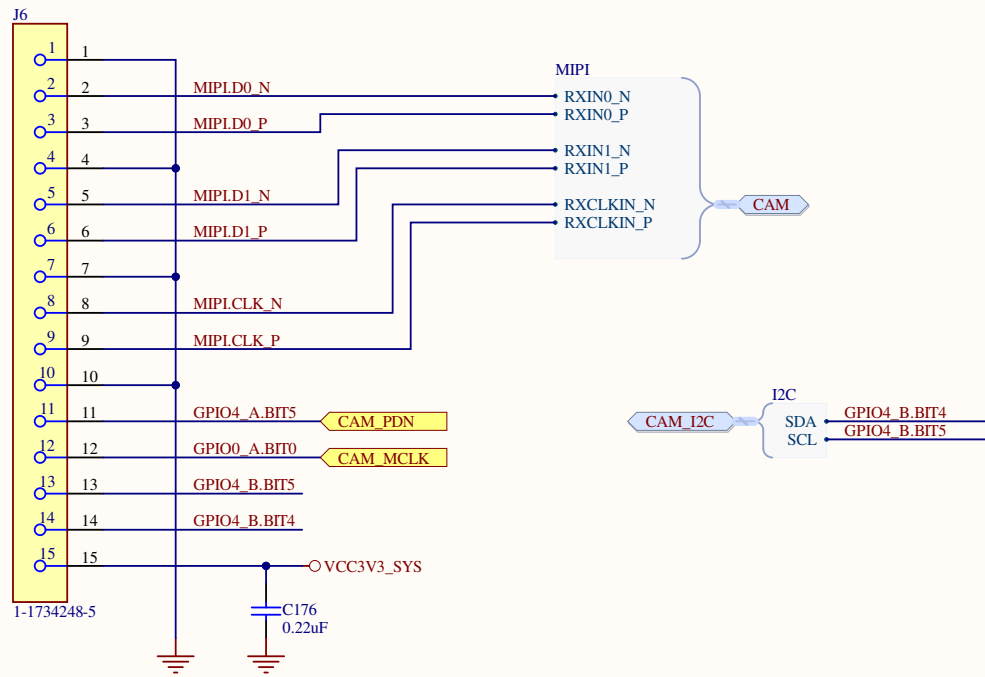
Title MCU RK3568			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 1.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 2 of 42			
File: RK3568.SchDoc					



Title Backlight Driver			Hardkernel Co.,LTD. 475-1 Manango Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 23.	Revision:		
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 3 of 42	Designed by: neal.kim@hardkernel.com	
File: BACKLIGHT_SGM3752.SchDoc				



Title Audio Jack			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 20.	Revision: 0.3			
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 4 of 42			
File: CON_AUDIO.SchDoc			Designed by: *@hardkernel.com		



Title MIPI CAMERA CONNECTOR			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 1.	Revision: 0.1		
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 5 of 42		
File: CON_CAMERA_MIPI.SchDoc			Designed by: ruppi kim@hardkernel.com	

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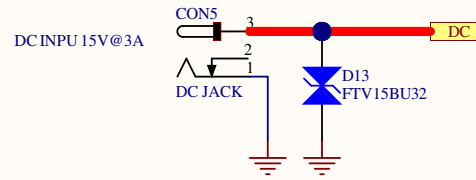
B

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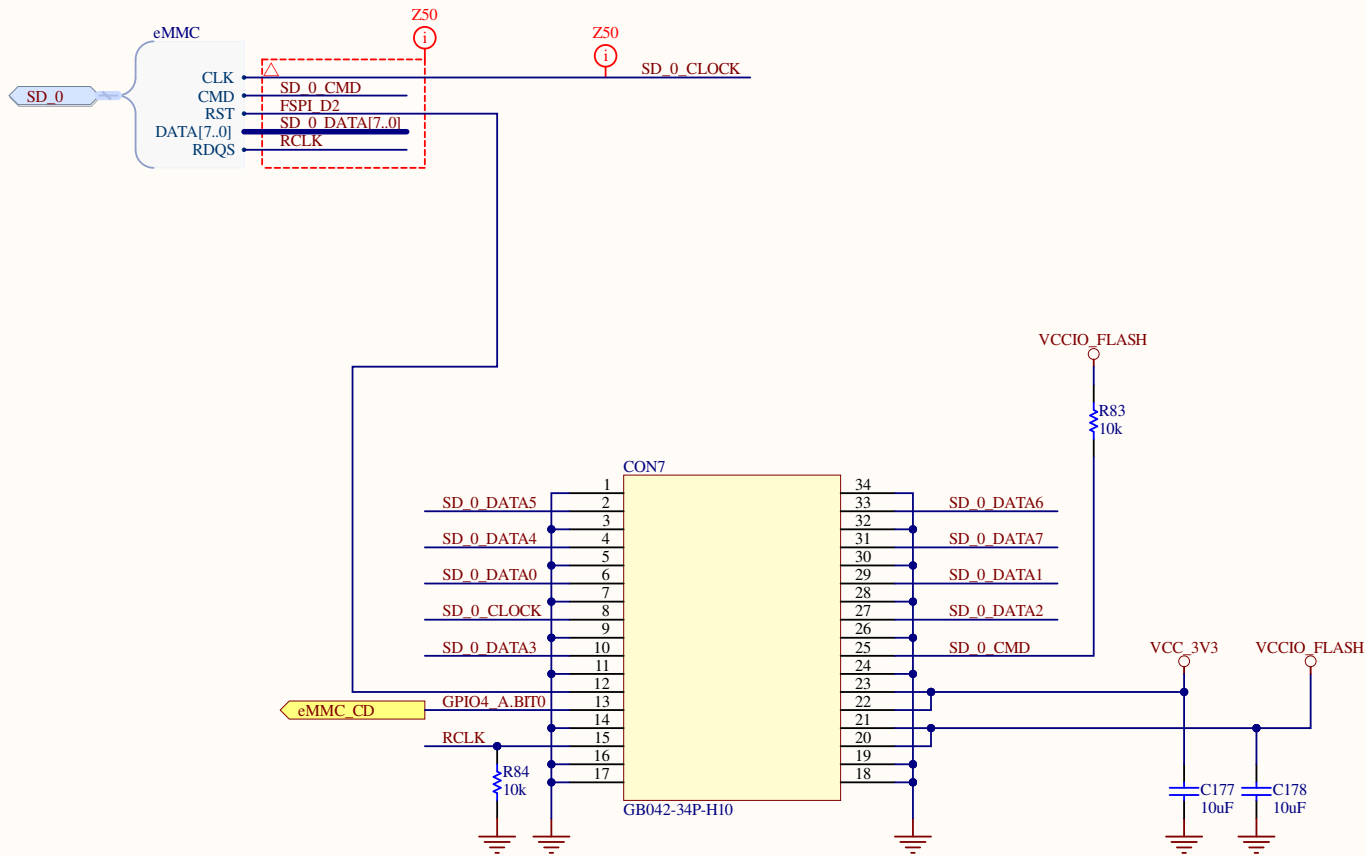
Title DC Jack			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 22.	Revision: 0.1			
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 6 of 42			
File: CON_DCJACK.SchDoc			Designed by: ruppi kim@hardkernel.com		

1

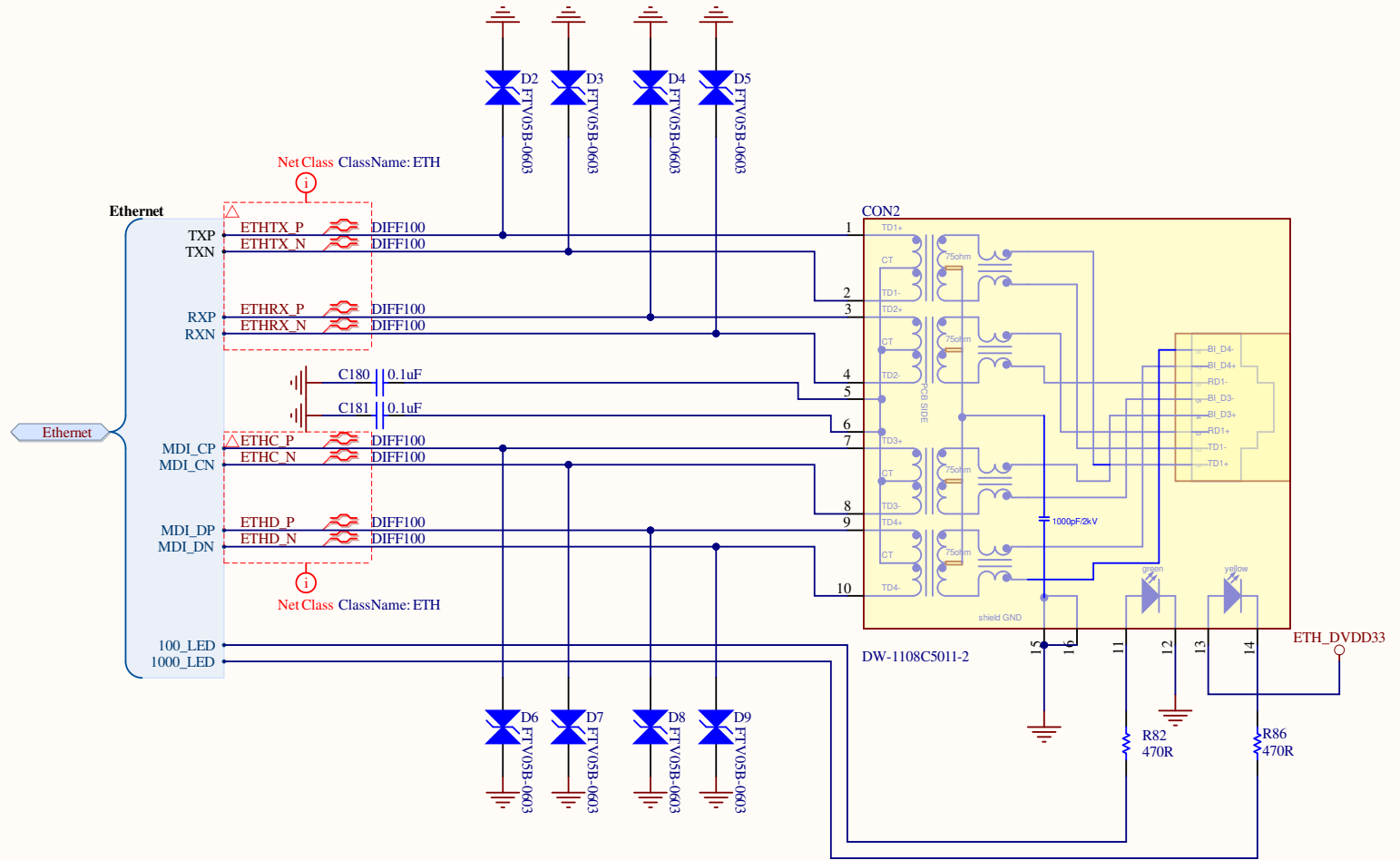
2

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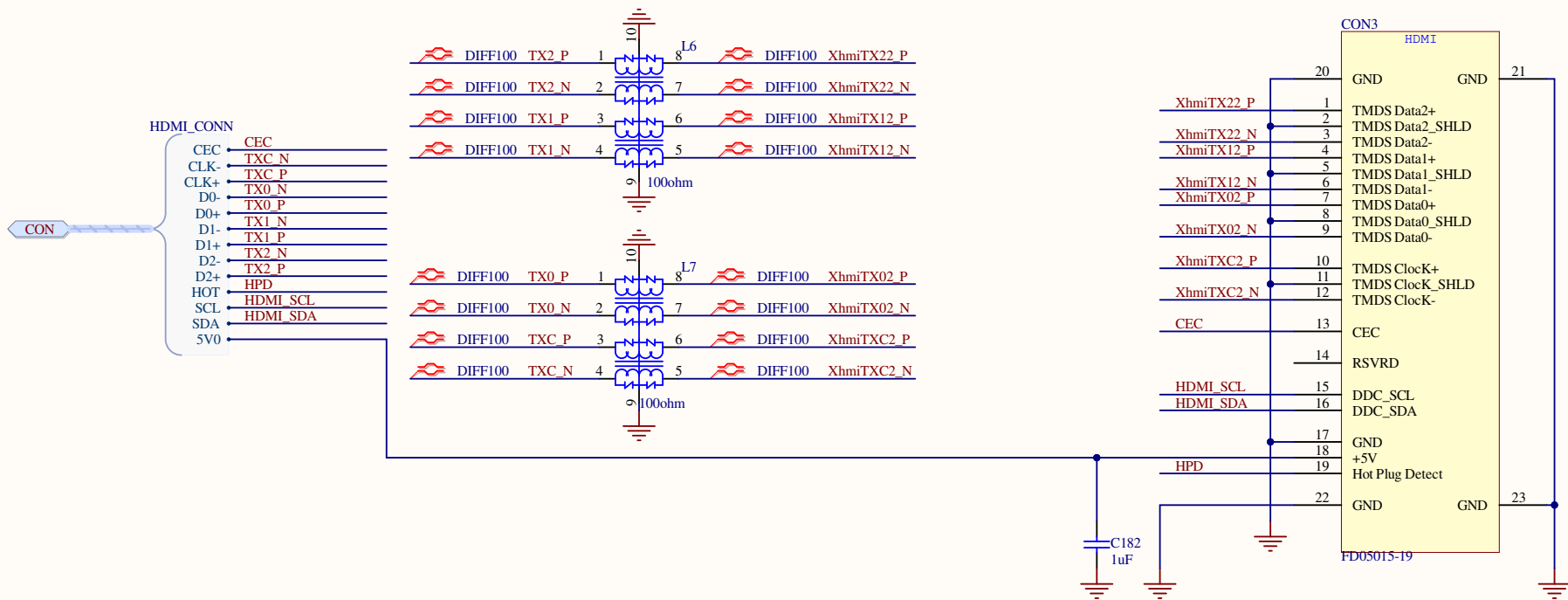
4



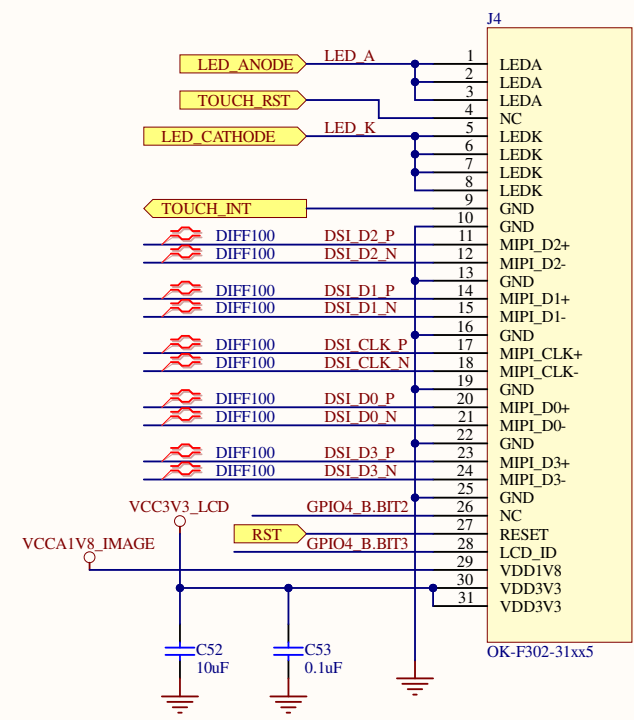
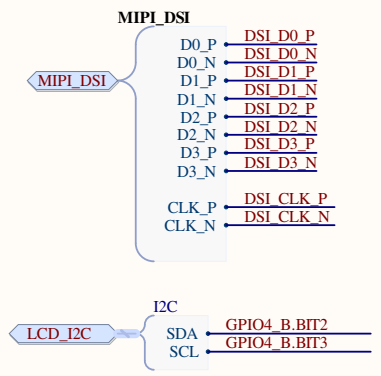
Title eMMC Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 29.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:19 PM	Sheet 7 of 42			
File: CON_EMMC.SchDoc					



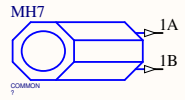
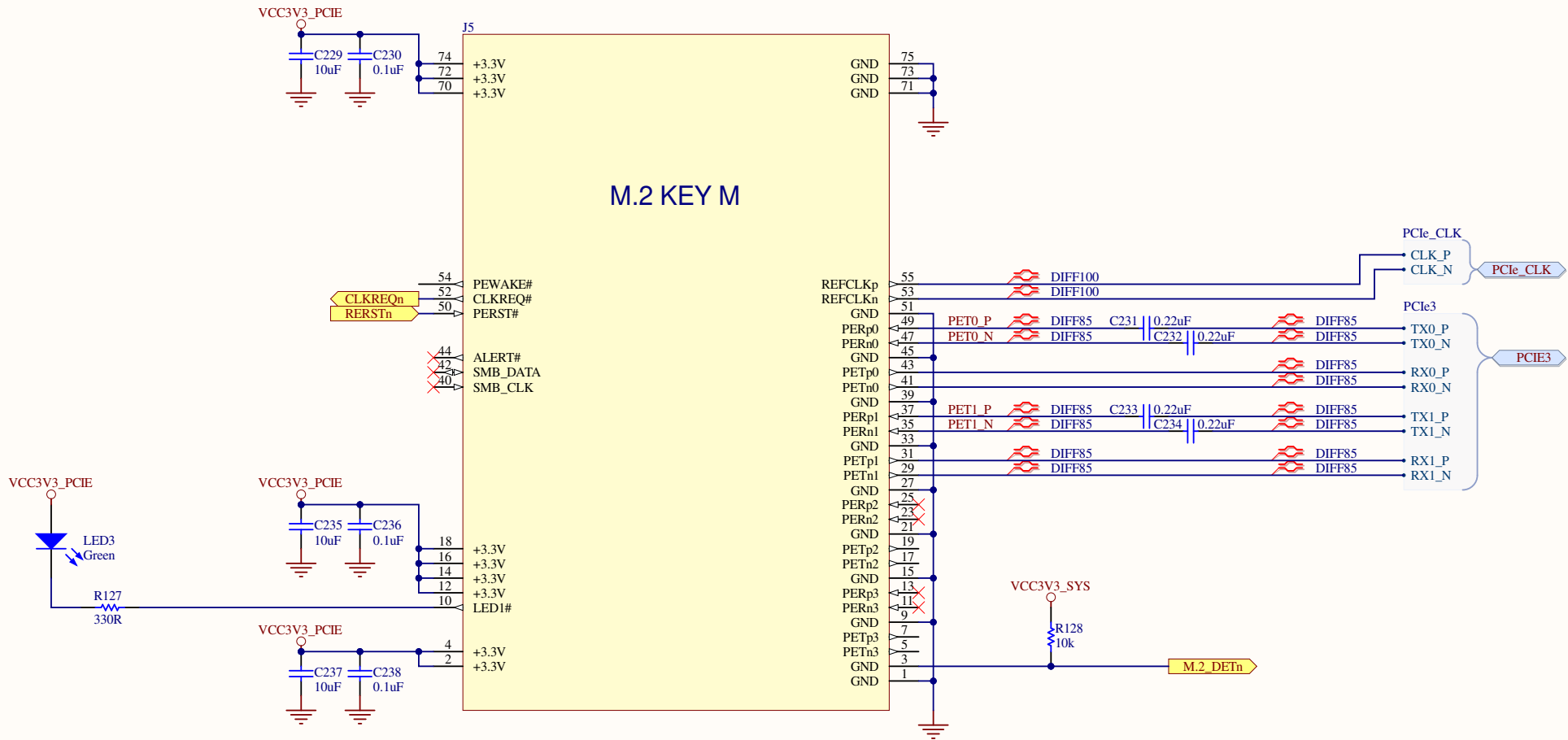
Title Giga Ethernet Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea Designed by: ruppi.kim@hardkernel.com	
Size: A4	Number: 22.	Revision: 0.1		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 8 of 42		
File: CON_GIGA_ETH.SchDoc				



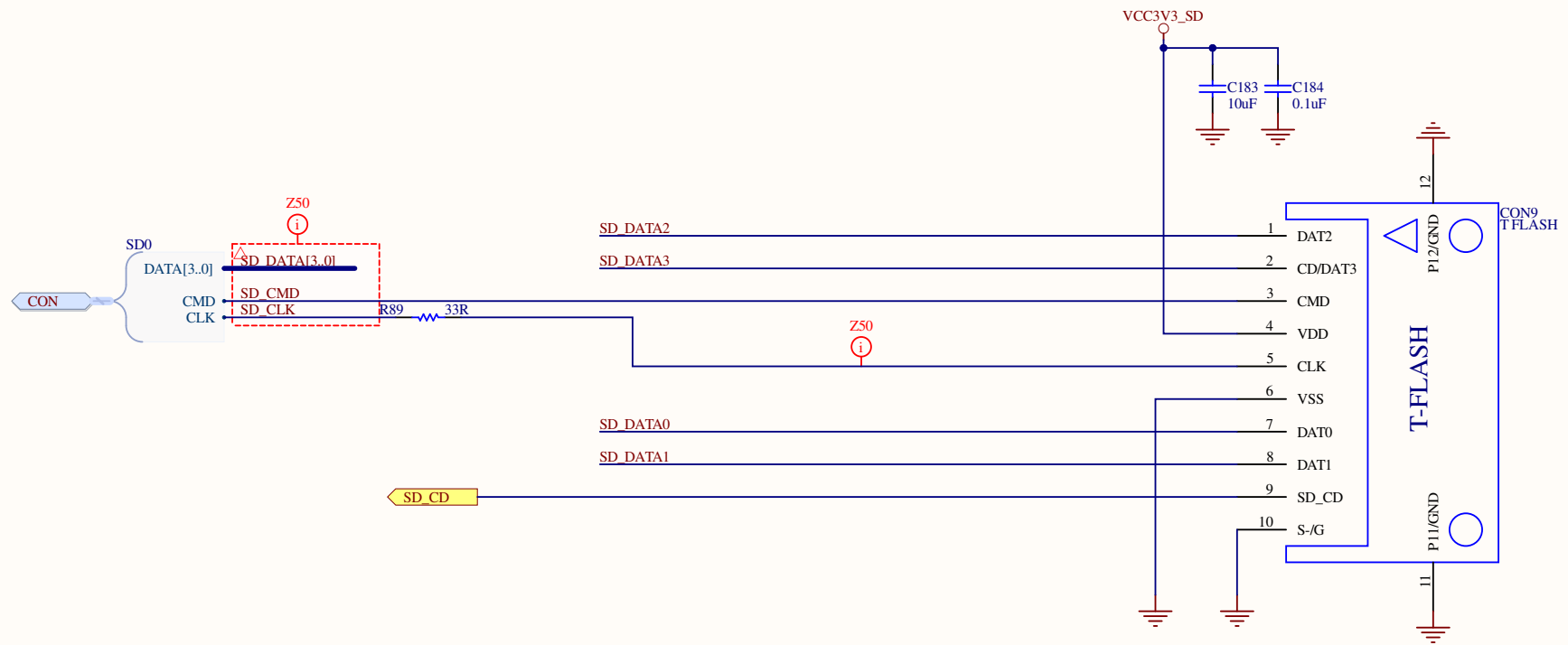
Title HDMI Type A Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 1.	Revision: 0.1	Designed by: ruppi.kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 9 of 42			
File: CON_HDMI.SchDoc					



Title CON_LCD_KD50T048-A			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 16.	Revision: 1.0		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 10 of 42	Designed by: *@hardkernel.com	
File: CON_LCD_KD50T048-A_MIP1.SchDoc				



Title M.2 KEY M Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 21.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 11 of 42			
File: CON_M2.SchDoc					



Title Micro SD Socket			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 24.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 12 of 42		
File: CON_MICROSD_HD08-AL00335.SchDoc				

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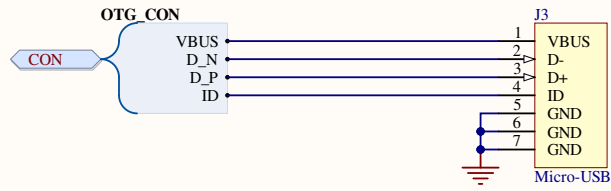
B

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Title Micro USB Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 31.	Revision: 0.1			
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 13 of 42			
File: CON_MicroUSB.SchDoc			Designed by: ruppi.kim@hardkernel.com		

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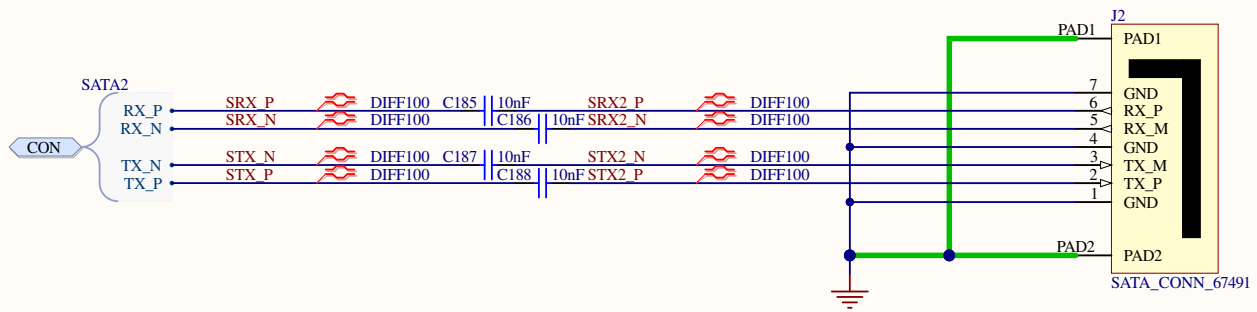
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Title SATA Connector			Hardkernel Co., LTD. 1-605 Shinan Metrokhan 1115 Dalandong, Dongangu, Anyang, Gyeonggido South Korea	
Size: A4	Number: 8.	Revision: 0.1		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 14 of 42		
File: CON_SATA.SchDoc			Designed by: *	

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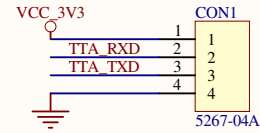
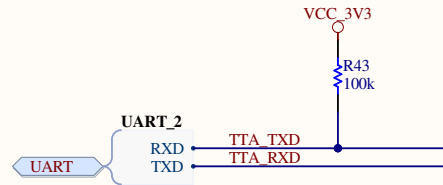
B

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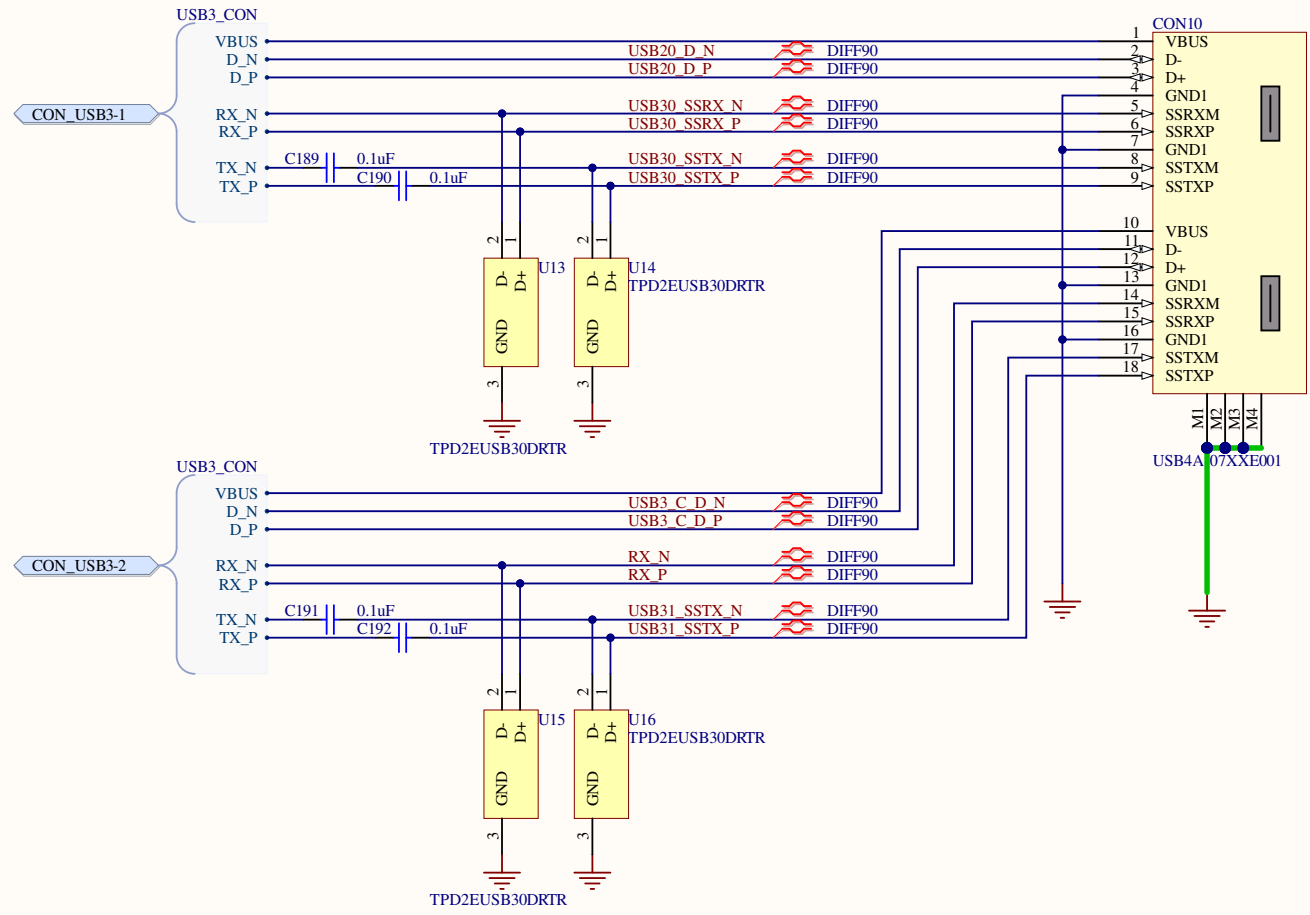
Title UART Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 1.	Revision: 0.1	Designed by: ruppi.kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 15 of 42			
File: CON_UART.SchDoc					

1

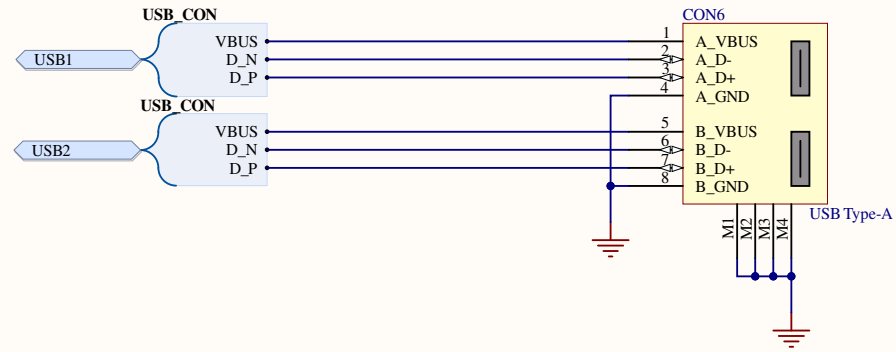
2

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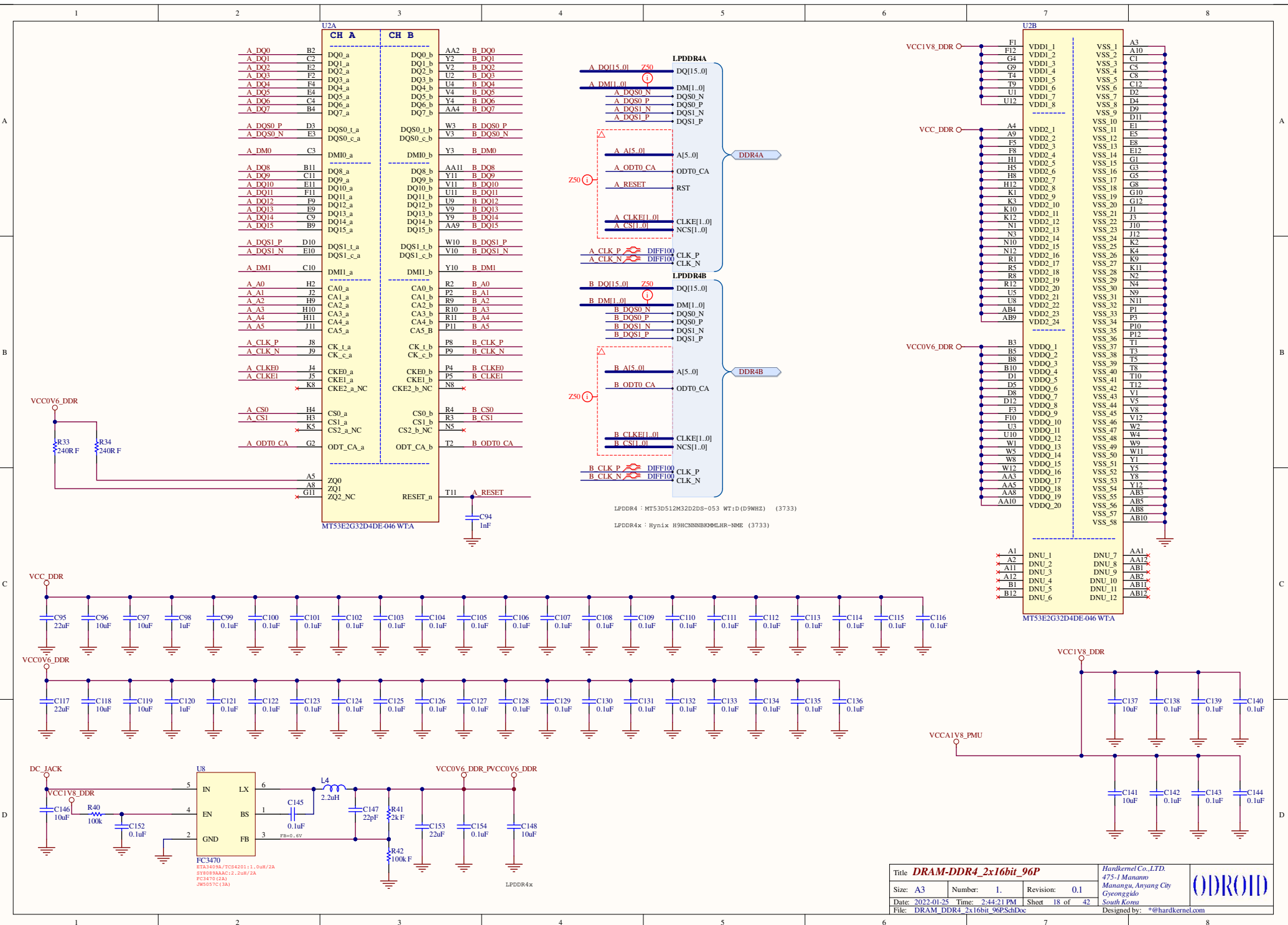
4



Title USB 3.0 Type A Connector			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 15.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:20 PM	Sheet 16 of 42		
File: CON_USB3_DUAL_RA.SchDoc				

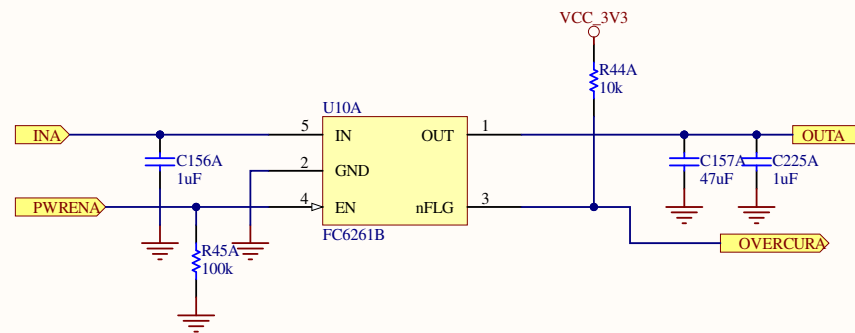


Title USB 2.0 Type A Connector			Hardkernel Co.,LTD. 1-605 Shinan Metrokhan 1115 Dalandong, Dongangu, Anyang, Gyeonggido South Korea	ODROID
Size: A4	Number: 20.	Revision: 0.3	Designed by: ruppi.kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:21 PM	Sheet 17 of 42		
File: CON_USB_RA.SchDoc				

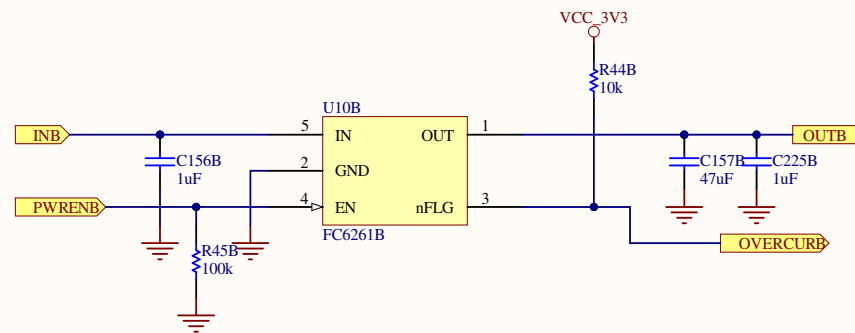


Title DRAM-DDR4_2x16bit_96P		Hardkernel Co., LTD.	
Size: A3		475-J Manann	
Number: 1.	Revision: 0.1	Manangu, Anyang City	
Date: 2022-01-25	Time: 2:44:21 PM	South Korea	
File: DRAM_DDR4_2x16bit_96P.SchDoc	Sheet 18 of 42	Designed by: *@hardkernel.com	

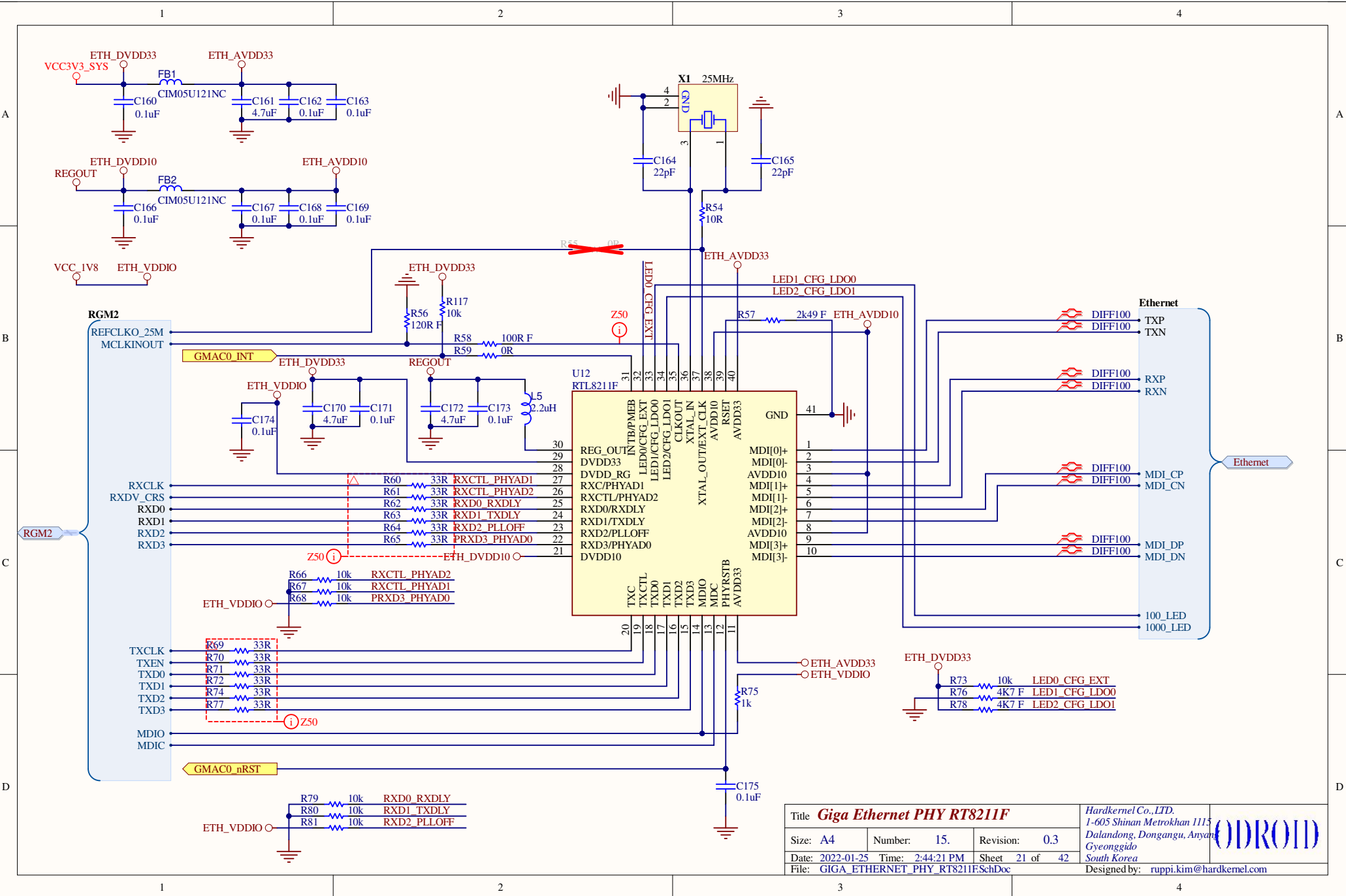




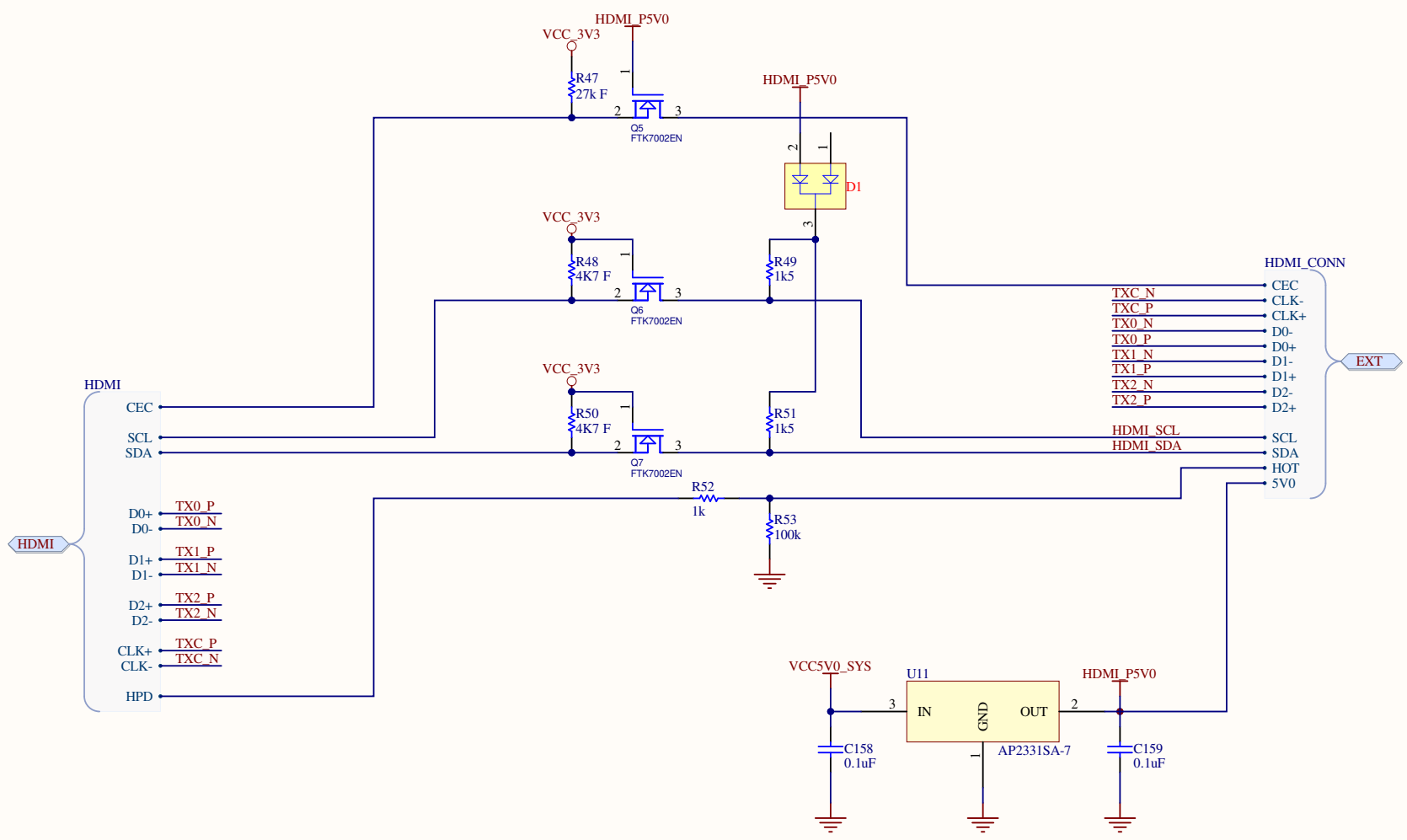
Title USB HOST Power Switch			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 16.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:21 PM	Sheet 19 of 42		
File: FC6261B.SchDoc				



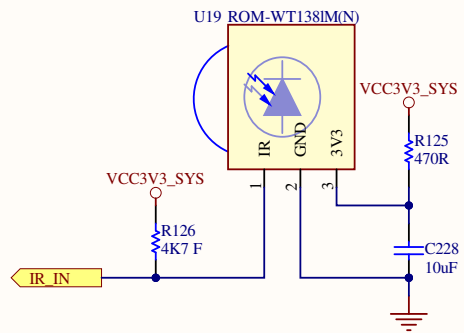
Title USB HOST Power Switch			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 16.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:21 PM	Sheet 20 of 42			
File: FC6261B.SchDoc					




Title Giga Ethernet PHY RT8211F			Hardkernel Co.,LTD. 1-605 Shinan Metrokhan 1115 Dalandong, Dongangu, Anyang, Gyeonggido South Korea	ODROID
Size: A4	Number: 15.	Revision: 0.3		
Date: 2022-01-25	Time: 2:44:21 PM	Sheet 21 of 42	Designed by: ruppi.kim@hardkernel.com	
File: GIGA_ETHERNET_PHY_RT8211F.SchDoc				



Title HDMI 2C			Hardkernel Co., LTD. 704 Anyang K-center 1591-9 Burim, Dongangju, Anyang Kyeonggido South Korea	
Size: A4	Number: 24.	Revision: 0.3	ODROID	
Date: 2022-01-25	Time: 2:44:21 PM	Sheet 22 of 42		
File: HDMI_12C.SchDoc			Designed by: ruppi.kim@hardkernel.com	



Title Remote Controller Receiver			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	
Size: A4	Number: 28.	Revision: 0.1		
Date: 2022-01-25	Time: 2:44:22 PM	Sheet 23 of 42	Designed by: ruppi.kim@hardkernel.com	
File: IR.SchDoc				

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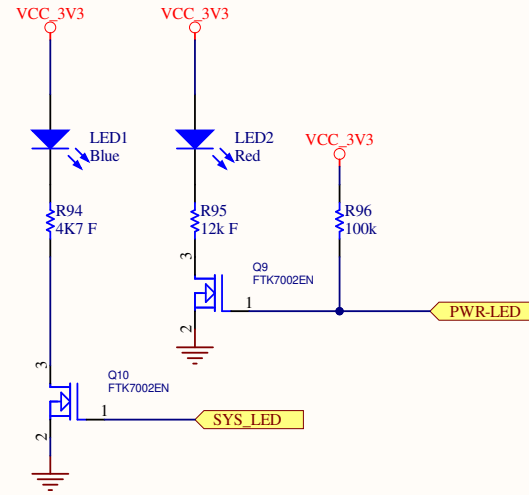
B

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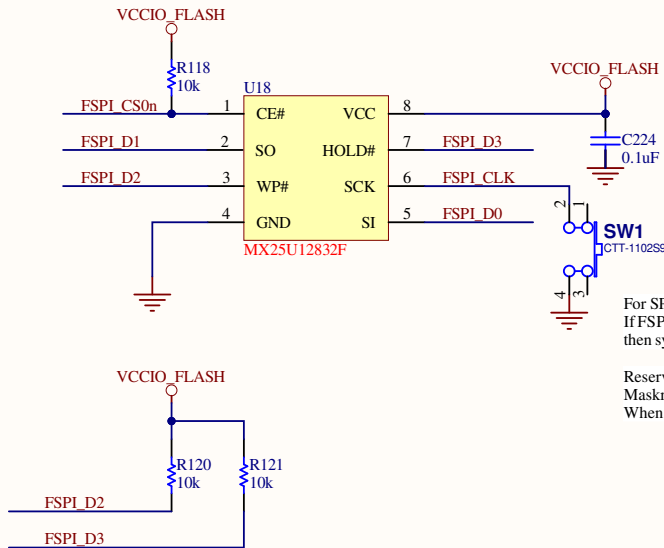
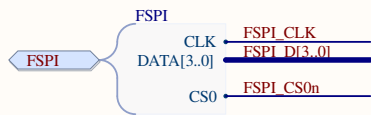
Title Indicator LEDs			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 25.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:22 PM	Sheet 24 of 42			
File: M1_LEDS.SchDoc					

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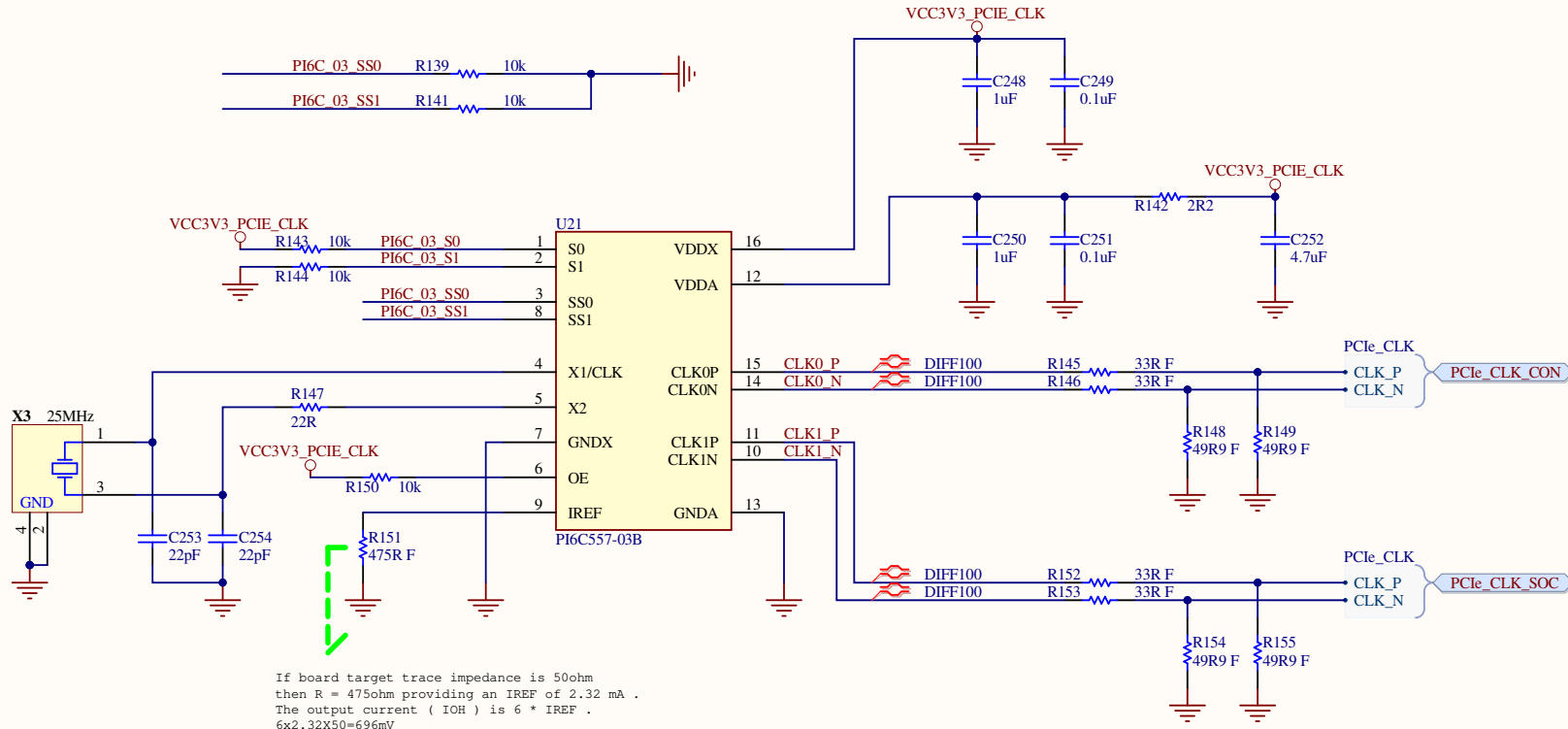
4



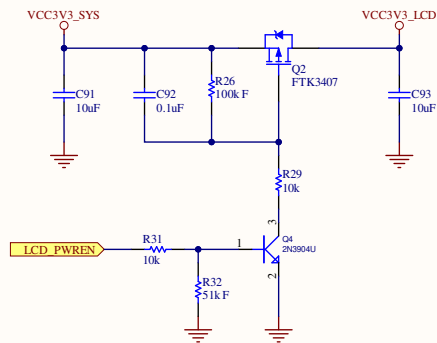
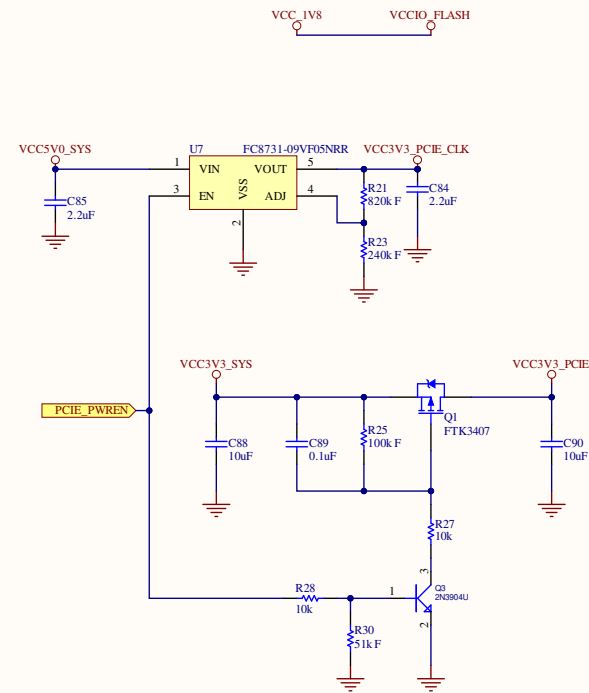
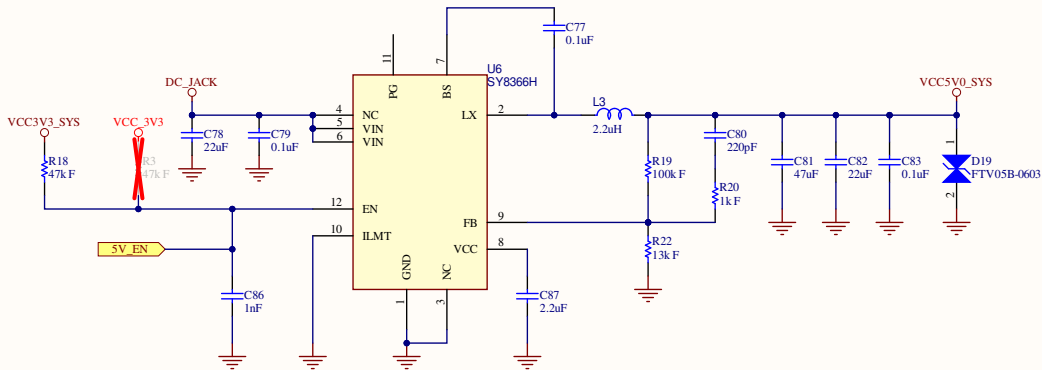
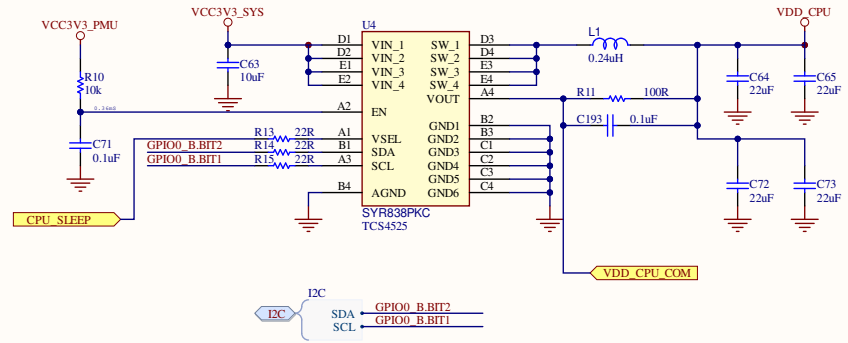
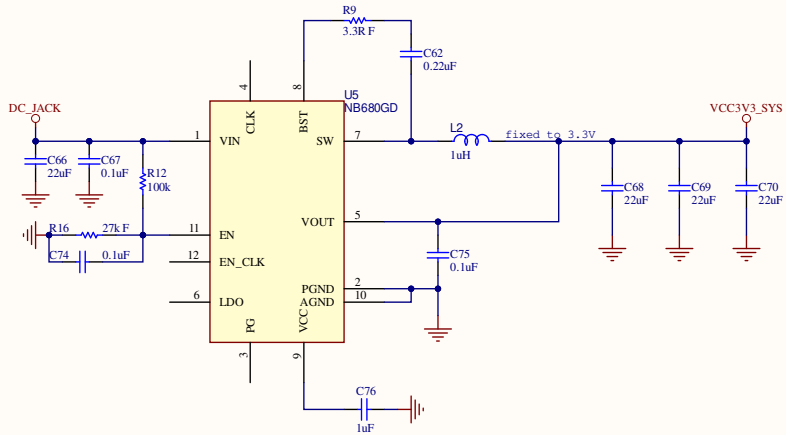
For SPI Flash:
If FSPI_CLK=0V at after power on and reset,
then system will enter into Maskrom mode.

Reserve test point for put the system into
Maskrom mode to update the firmware
When writing mismatched firmware or other

Title SPI FLash 128Mbit			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 1.	Revision: 0.1		
Date: 2022-01-25	Time: 2:44:22 PM	Sheet 25 of 42		
File: MEM_SPI_FLASH.SchDoc			Designed by: ruppi.kim@hardkernel.com	



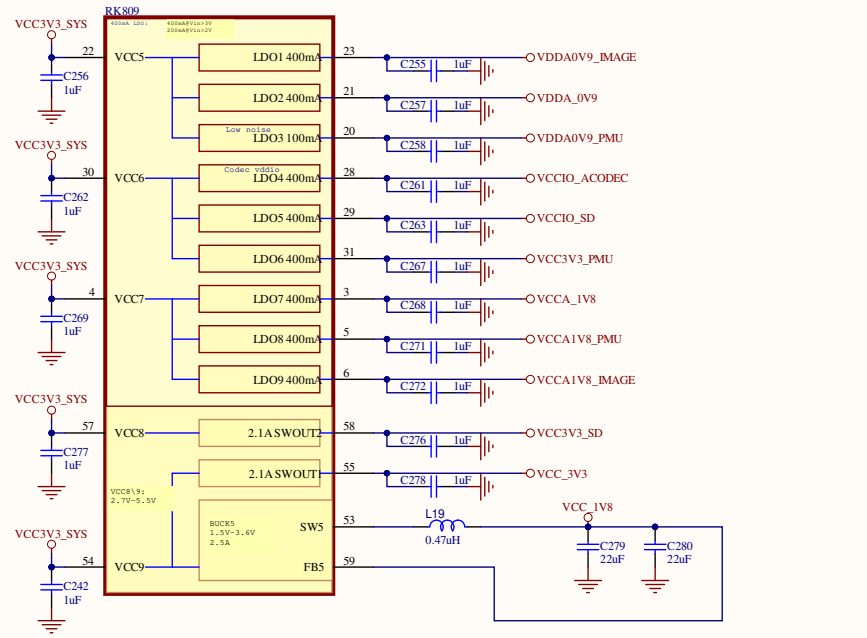
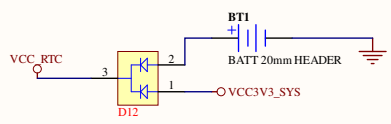
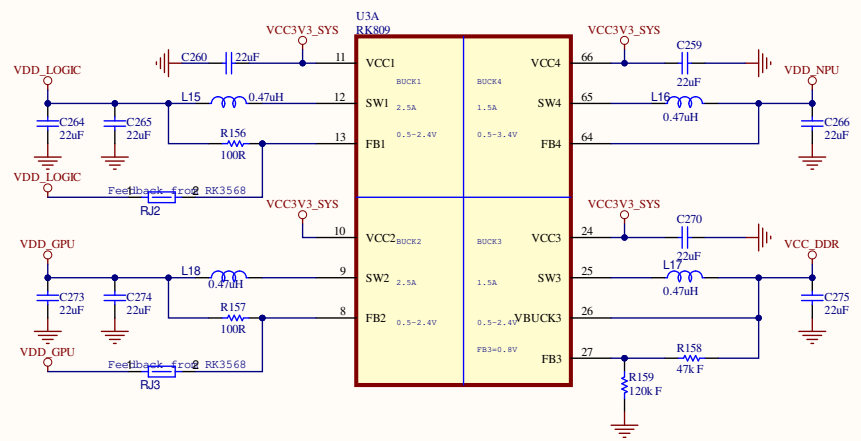
Title *			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 1.	Revision: 0.1	Designed by: *@hardkernel.com		
Date: 2022-01-25	Time: 2:44:22 PM	Sheet 26 of 42			
File: PCIe_CLK.SchDoc					



Title PWR DCDC CPU GPU			Handkernel Co., LTD.	ODROID
Size: A3			473-1 Manamno	
Number: 12.	Revision: 0.1	Date: 2022-01-25	Manangu, Anyang City	
Time: 2:44:22 PM	Sheet 27 of 42	File: PWR DCDC_CPU_GPU.SchDoc	Gyeonggdo	
Designed by: ruppi.kim@hardkernel.com			South Korea	

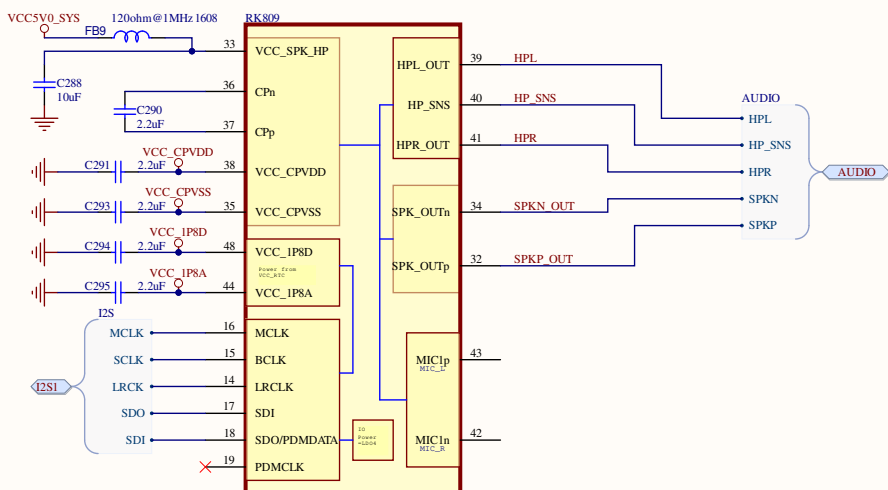
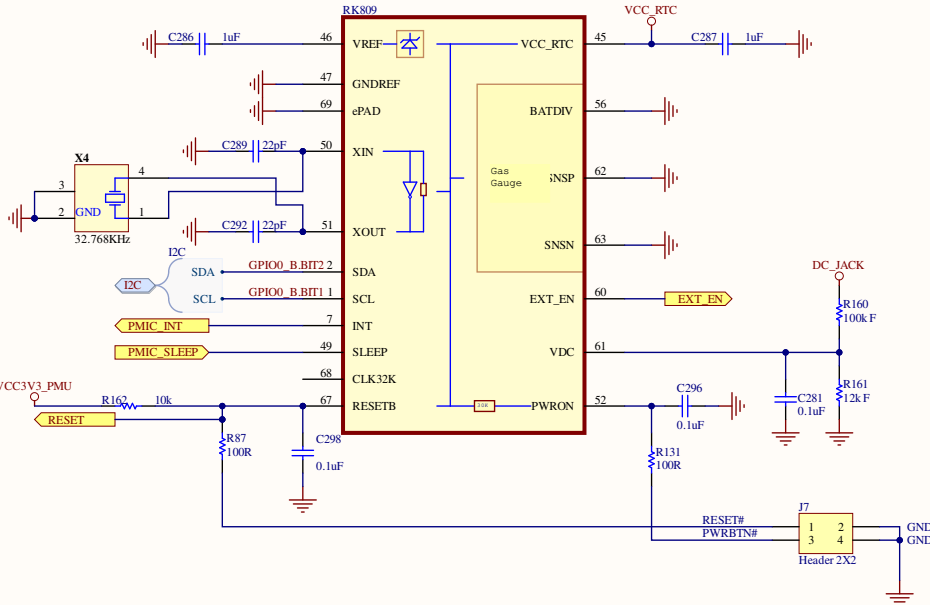
A

A



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C

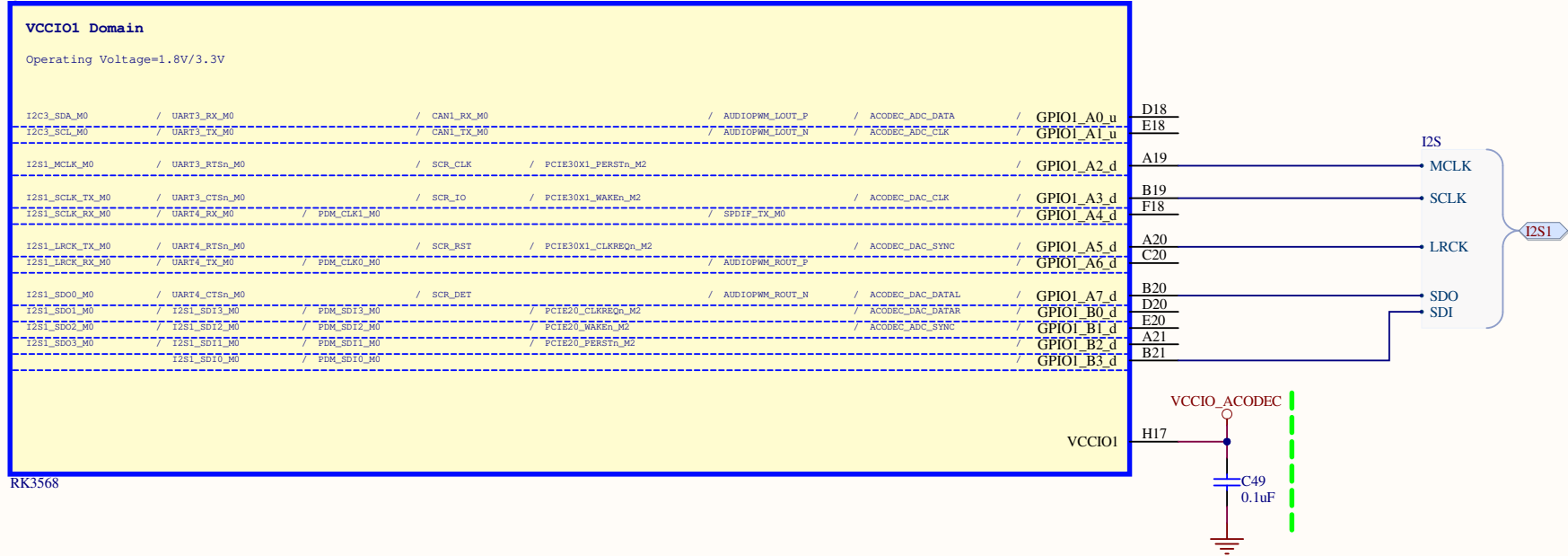
C

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RK3568_H (VCCIO1 Domain)

UIH



RK3568

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

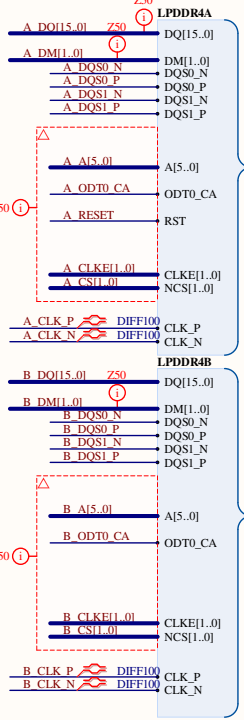
Title RK3568_Audio Interface			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea		ODROID
Size: A4	Number: 1.	Revision: 0.1	Designed by: ruppi.kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:22 PM	Sheet 29 of 42			
File: RK3568_Audio Interface.SchDoc					

RK3568_F (DDR PHY)

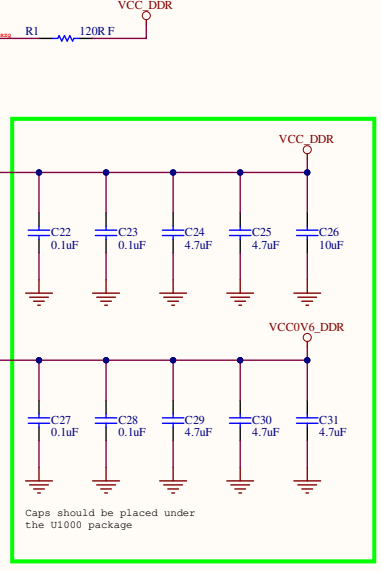
LUF

	DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3
A DQ0 F2	DDR_DQ0_A	DDR4_DQ0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ0	DDR4_A0	LPDDR4_CLKP_B	DDR3_A9
A DQ1 E1	DDR_DQ1_A	DDR4_DQ1_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ1	DDR4_A1	---	---
A DQ2 E2	DDR_DQ2_A	DDR4_DQ2_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ2	DDR4_A2	---	---
A DQ3 D1	DDR_DQ3_A	DDR4_DQ3_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ3	DDR4_A3	---	---
A DQ4 H1	DDR_DQ4_A	DDR4_DQ4_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ4	DDR4_A4	---	---
A DQ5 J2	DDR_DQ5_A	DDR4_DQ5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ5	DDR4_A5	---	---
A DQ6 H1	DDR_DQ6_A	DDR4_DQ6_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ6	DDR4_A6	---	---
A DQ7 H4	DDR_DQ7_A	DDR4_DQ7_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ7	DDR4_A7	---	---
A DM0 H5	DDR_DM0_A	DDR4_DM0_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM0	DDR4_A8	---	---
A DQSO_P G1	DDR_DQSO_P_A	DDR4_DQSO_P_A	LPDDR4_DQSO_P_A	DDR3_DQSO_P	LPDDR3_DQSO_P	DDR4_A9	---	---
A DQSO_N G2	DDR_DQSO_N_A	DDR4_DQSO_N_A	LPDDR4_DQSO_N_A	DDR3_DQSO_N	LPDDR3_DQSO_N	DDR4_A10	---	---
A DQ8 M1	DDR_DQ8_A	DDR4_DQ8_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ8	DDR4_A11	---	---
A DQ9 N2	DDR_DQ9_A	DDR4_DQ9_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ9	DDR4_A12	---	---
A DQ10 L7	DDR_DQ10_A	DDR4_DQ10_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ10	DDR4_A13	---	---
A DQ11 L6	DDR_DQ11_A	DDR4_DQ11_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ11	DDR4_A14	---	---
A DQ12 K2	DDR_DQ12_A	DDR4_DQ12_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ12	DDR4_A15	---	---
A DQ13 J6	DDR_DQ13_A	DDR4_DQ13_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ13	DDR4_A16	---	---
A DQ14 A	DDR_DQ14_A	DDR4_DQ14_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ14	DDR4_A17	---	---
A DQ15 L4	DDR_DQ15_A	DDR4_DQ15_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ15	DDR4_A18	---	---
A DM1 J4	DDR_DM1_A	DDR4_DM1_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM1	DDR4_A19	---	---
A DQSI_P L2	DDR_DQSI_P_A	DDR4_DQSI_P_A	LPDDR4_DQSI_P_A	DDR3_DQSI_P	LPDDR3_DQSI_P	DDR4_B0	---	---
A DQSI_N L1	DDR_DQSI_N_A	DDR4_DQSI_N_A	LPDDR4_DQSI_N_A	DDR3_DQSI_N	LPDDR3_DQSI_N	DDR4_B1	---	---
B DQ0 B10	DDR_DQ0_B	DDR4_DQ0_B	LPDDR4_DQ0_B	DDR3_DQ0	LPDDR3_DQ0	DDR4_B2	---	---
B DQ1 A9	DDR_DQ1_B	DDR4_DQ1_B	LPDDR4_DQ1_B	DDR3_DQ1	LPDDR3_DQ1	DDR4_B3	---	---
B DQ2 D12	DDR_DQ2_B	DDR4_DQ2_B	LPDDR4_DQ2_B	DDR3_DQ2	LPDDR3_DQ2	DDR4_B4	---	---
B DQ3 E12	DDR_DQ3_B	DDR4_DQ3_B	LPDDR4_DQ3_B	DDR3_DQ3	LPDDR3_DQ3	DDR4_B5	---	---
B DQ4 A12	DDR_DQ4_B	DDR4_DQ4_B	LPDDR4_DQ4_B	DDR3_DQ4	LPDDR3_DQ4	DDR4_B6	---	---
B DQ5 D15	DDR_DQ5_B	DDR4_DQ5_B	LPDDR4_DQ5_B	DDR3_DQ5	LPDDR3_DQ5	DDR4_B7	---	---
B DQ6 E15	DDR_DQ6_B	DDR4_DQ6_B	LPDDR4_DQ6_B	DDR3_DQ6	LPDDR3_DQ6	DDR4_B8	---	---
B DQ7 E14	DDR_DQ7_B	DDR4_DQ7_B	LPDDR4_DQ7_B	DDR3_DQ7	LPDDR3_DQ7	DDR4_B9	---	---
B DM0 D14	DDR_DM0_B	DDR4_DM0_B	LPDDR4_DM0_B	DDR3_DM0	LPDDR3_DM0	DDR4_B10	---	---
B DQSO_P A11	DDR_DQSO_P_B	DDR4_DQSO_P_B	LPDDR4_DQSO_P_B	DDR3_DQSO_P	LPDDR3_DQSO_P	DDR4_B11	---	---
B DQSO_N B11	DDR_DQSO_N_B	DDR4_DQSO_N_B	LPDDR4_DQSO_N_B	DDR3_DQSO_N	LPDDR3_DQSO_N	DDR4_B12	---	---
B DQ8 A16	DDR_DQ8_B	DDR4_DQ8_B	LPDDR4_DQ8_B	DDR3_DQ8	LPDDR3_DQ8	DDR4_B13	---	---
B DQ9 B17	DDR_DQ9_B	DDR4_DQ9_B	LPDDR4_DQ9_B	DDR3_DQ9	LPDDR3_DQ9	DDR4_B14	---	---
B DQ10 A17	DDR_DQ10_B	DDR4_DQ10_B	LPDDR4_DQ10_B	DDR3_DQ10	LPDDR3_DQ10	DDR4_B15	---	---
B DQ11 B18	DDR_DQ11_B	DDR4_DQ11_B	LPDDR4_DQ11_B	DDR3_DQ11	LPDDR3_DQ11	DDR4_B16	---	---
B DQ12 B13	DDR_DQ12_B	DDR4_DQ12_B	LPDDR4_DQ12_B	DDR3_DQ12	LPDDR3_DQ12	DDR4_B17	---	---
B DQ13 A13	DDR_DQ13_B	DDR4_DQ13_B	LPDDR4_DQ13_B	DDR3_DQ13	LPDDR3_DQ13	DDR4_B18	---	---
B DQ14 D17	DDR_DQ14_B	DDR4_DQ14_B	LPDDR4_DQ14_B	DDR3_DQ14	LPDDR3_DQ14	DDR4_B19	---	---
B DQ15 B14	DDR_DQ15_B	DDR4_DQ15_B	LPDDR4_DQ15_B	DDR3_DQ15	LPDDR3_DQ15	DDR4_B20	---	---
B DM1 E17	DDR_DM1_B	DDR4_DM1_B	LPDDR4_DM1_B	DDR3_DM1	LPDDR3_DM1	DDR4_B21	---	---
B DQSI_P B15	DDR_DQSI_P_B	DDR4_DQSI_P_B	LPDDR4_DQSI_P_B	DDR3_DQSI_P	LPDDR3_DQSI_P	DDR4_B22	---	---
B DQSI_N A15	DDR_DQSI_N_B	DDR4_DQSI_N_B	LPDDR4_DQSI_N_B	DDR3_DQSI_N	LPDDR3_DQSI_N	DDR4_B23	---	---
P5	DDR_ECC_DQ0	DDR4_ECC_DQ0	---	DDR3_ECC_DQ0	---	DDR4_B24	---	---
M4	DDR_ECC_DQ1	DDR4_ECC_DQ1	---	DDR3_ECC_DQ1	---	DDR4_B25	---	---
M5	DDR_ECC_DQ2	DDR4_ECC_DQ2	---	DDR3_ECC_DQ2	---	DDR4_B26	---	---
M5	DDR_ECC_DQ3	DDR4_ECC_DQ3	---	DDR3_ECC_DQ3	---	DDR4_B27	---	---
R7	DDR_ECC_DQ4	DDR4_ECC_DQ4	---	DDR3_ECC_DQ4	---	DDR4_B28	---	---
P4	DDR_ECC_DQ5	DDR4_ECC_DQ5	---	DDR3_ECC_DQ5	---	DDR4_B29	---	---
R4	DDR_ECC_DQ6	DDR4_ECC_DQ6	---	DDR3_ECC_DQ6	---	DDR4_B30	---	---
P7	DDR_ECC_DM	DDR4_ECC_DM	---	DDR3_ECC_DM	---	DDR4_B31	---	---
P2	DDR_ECC_DQSO_P	DDR4_ECC_DQSO_P	---	DDR3_ECC_DQSO_P	---	DDR4_B32	---	---
P1	DDR_ECC_DQSO_N	DDR4_ECC_DQSO_N	---	DDR3_ECC_DQSO_N	---	DDR4_B33	---	---

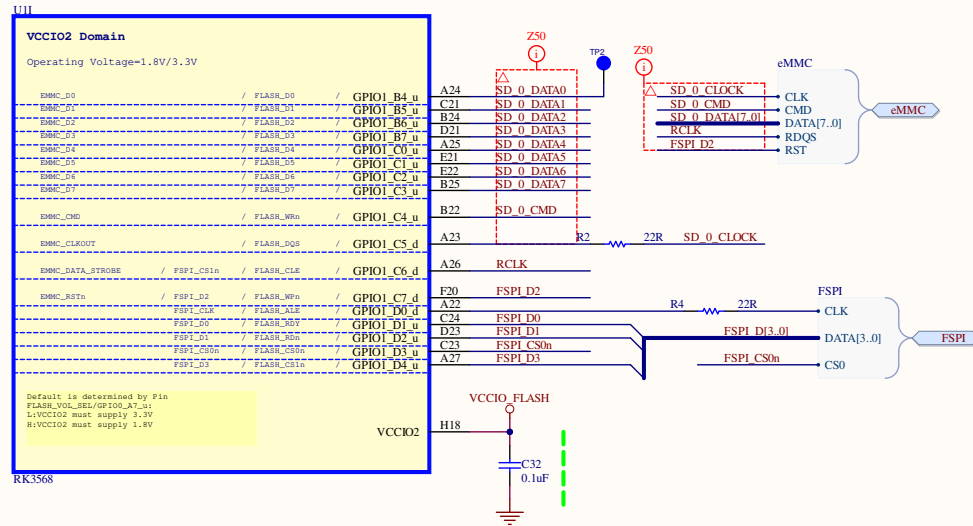
B6	B CLK P
F5	---
B1	A A1
F4	A CLKE1
D9	B A3
B7	B A5
A7	B A1
A8	B ODTU CA
C1	A ODTU CA
A5	B CLK N
D6	B CLKE0
C2	A A0
C4	A A3
B8	B A0
CS	A A4
E4	A A2
D5	A A5
E1	B A2
E9	B A4
F8	---
F7	---
B3	A CLKE0
B4	A CLK P
A4	A CLK N
A2	A CS0
B2	A CS1
B8	B CS1
D8	B CS0
F11	A RESET



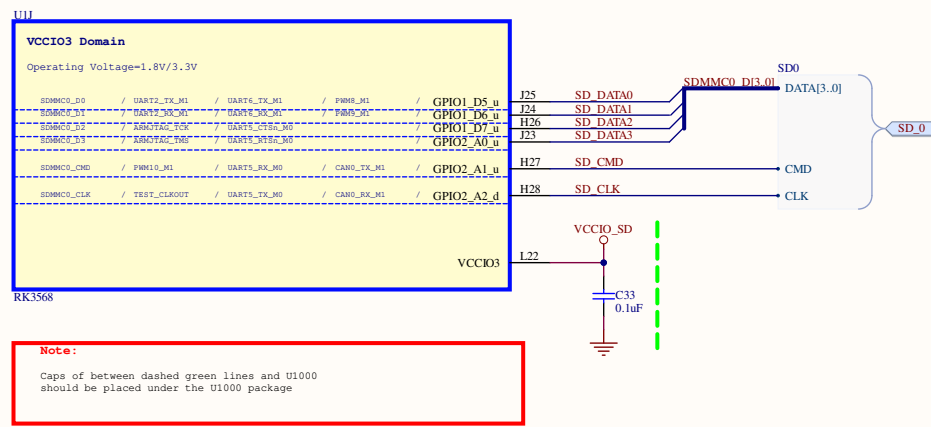
DDR3L	+1.35V	DDRPHY_VDDQ_1
DDR4	+1.2V	DDRPHY_VDDQ_2
LPDDR3	+1.2V	DDRPHY_VDDQ_3
LPDDR4	+1.1V	DDRPHY_VDDQ_4
LPDDR4x	+1.1V	DDRPHY_VDDQ_5
		DDRPHY_VDDQ_6
		DDRPHY_VDDQ_7
		DDRPHY_VDDQ_8
DDR3L	+1.35V	DDRPHY_VDDQL_1
DDR3	+1.5V	DDRPHY_VDDQL_2
DDR4	+1.2V	DDRPHY_VDDQL_3
LPDDR3	+1.2V	DDRPHY_VDDQL_4
LPDDR4	+1.1V	DDRPHY_VDDQL_5
LPDDR4x	#NAME?	DDRPHY_VDDQL_6



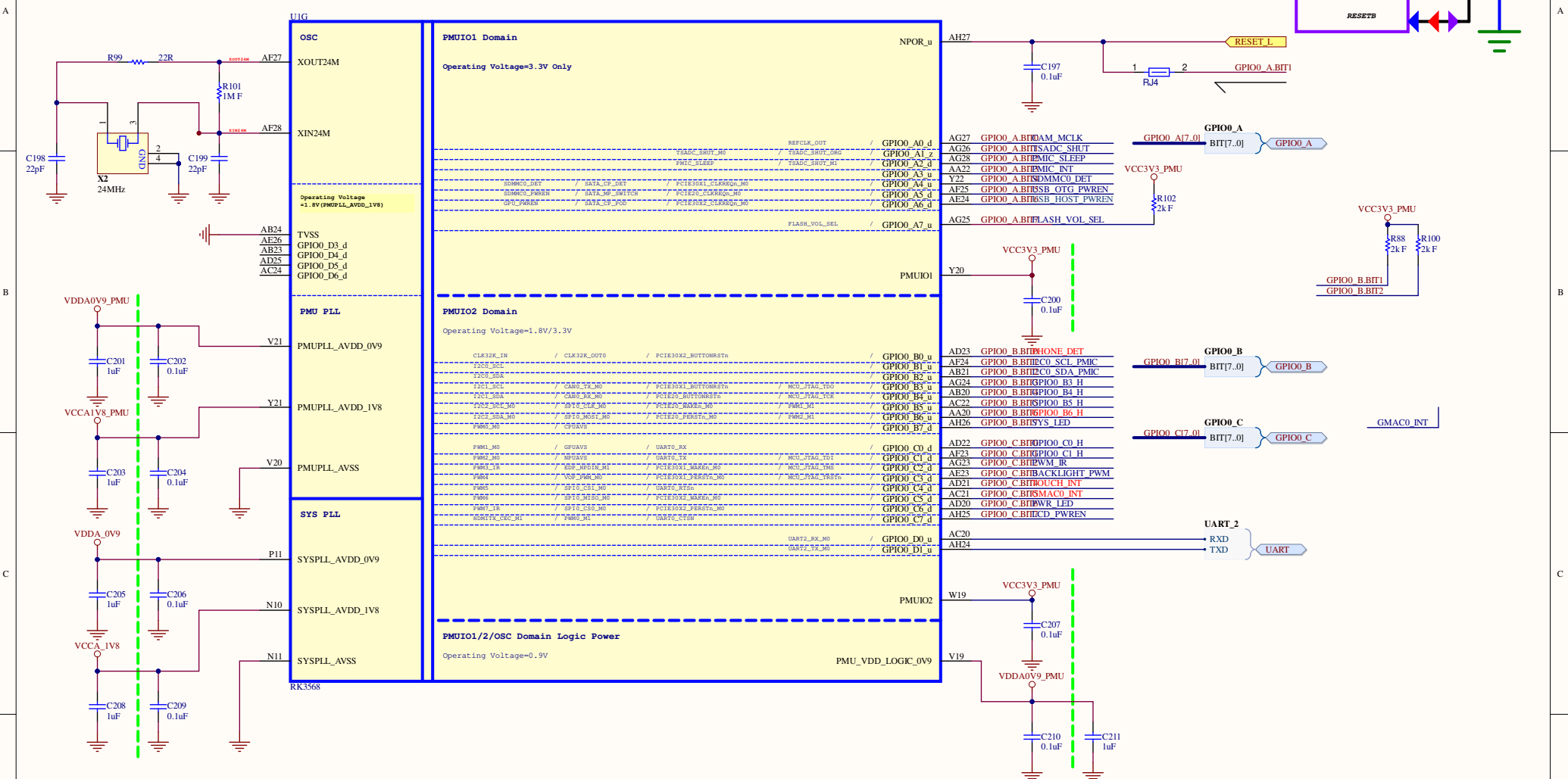
RK3568_I (VCCIO2 Domain)



RK3568_J (VCCIO3 Domain)



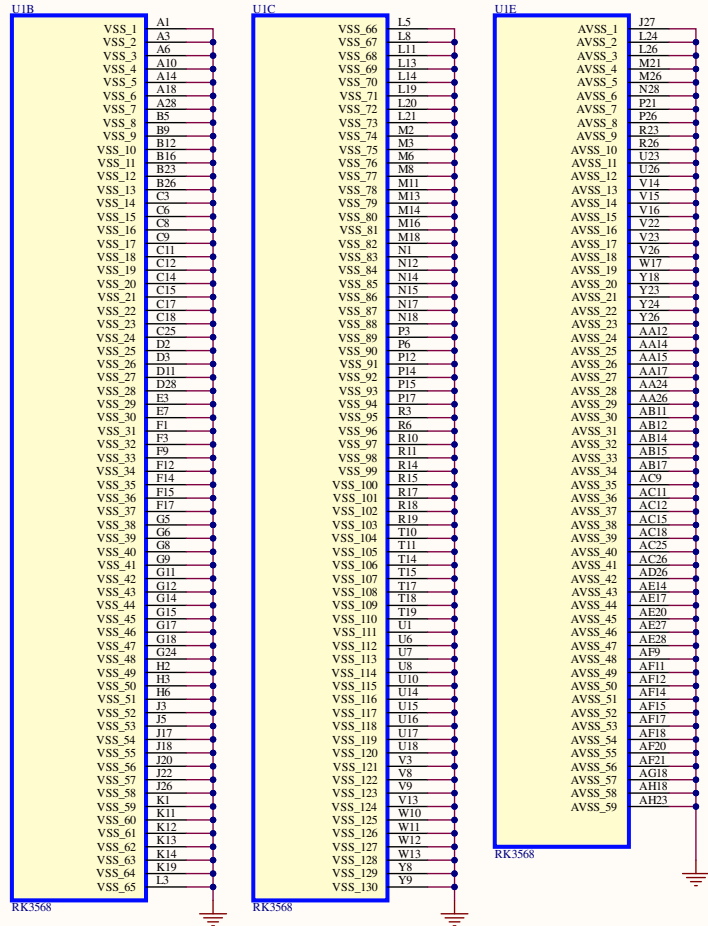
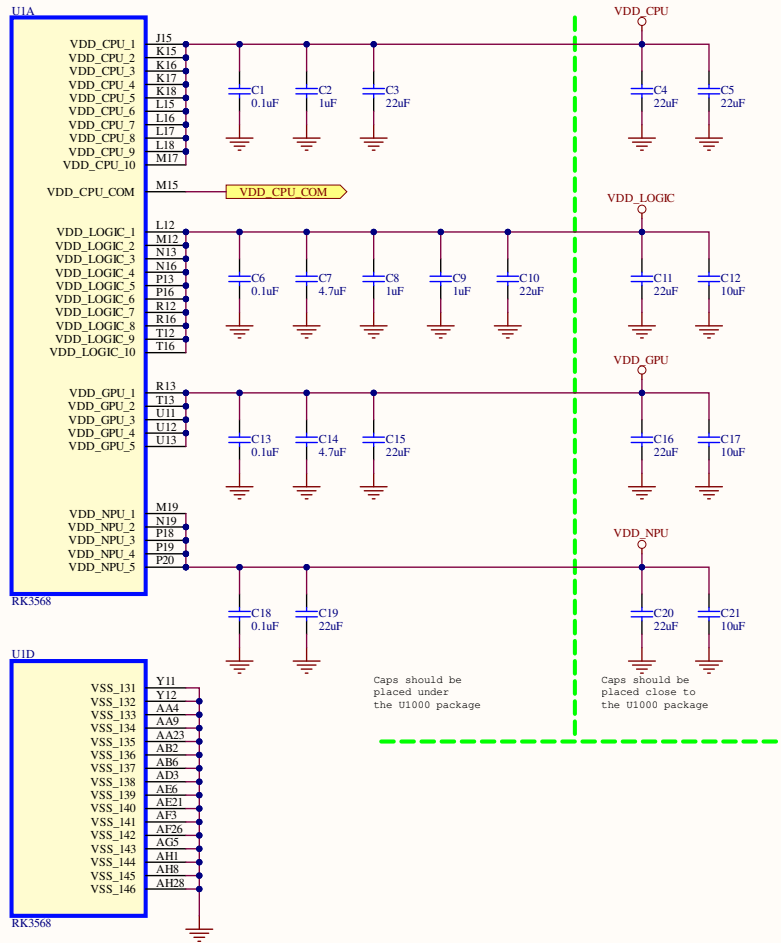
RK3568_G (OSC/PLL/PMUI01/2)



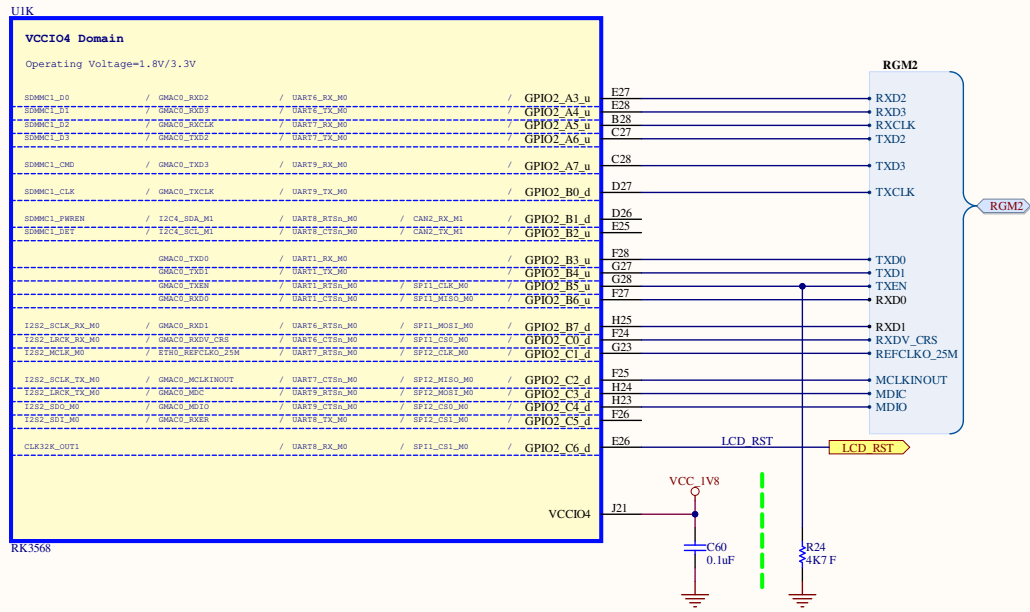
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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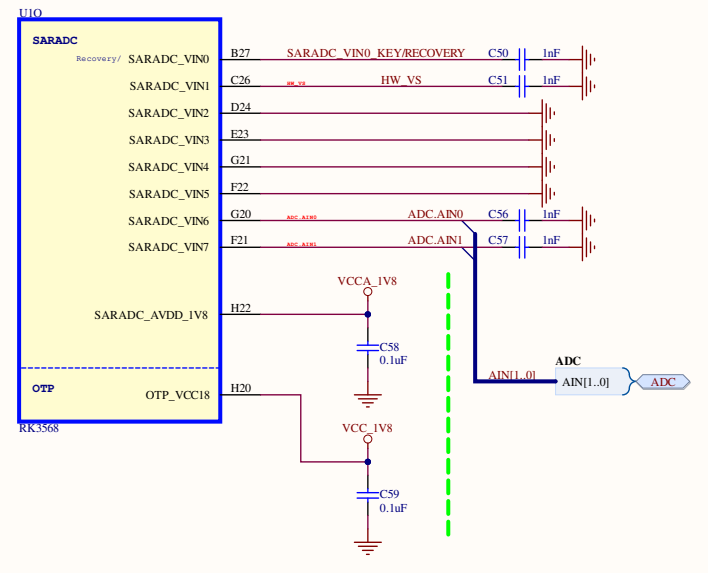
RK3568_ABCDE (Power&Gnd)



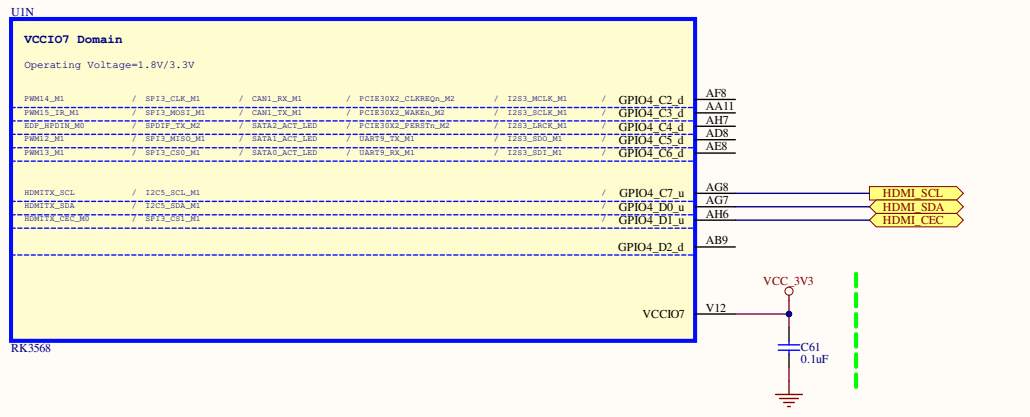
RK3568_K (VCCIO4 Domain)



RK3568_O (SARADC/OTP)



RK3568_N (VCCIO7 Domain)



Note: Must be mounted

VCCA_IV8 R7 91kF

SARADC_VIN0_KEY/RECOVERY R6 10k TP7 TP_SMD_0.5

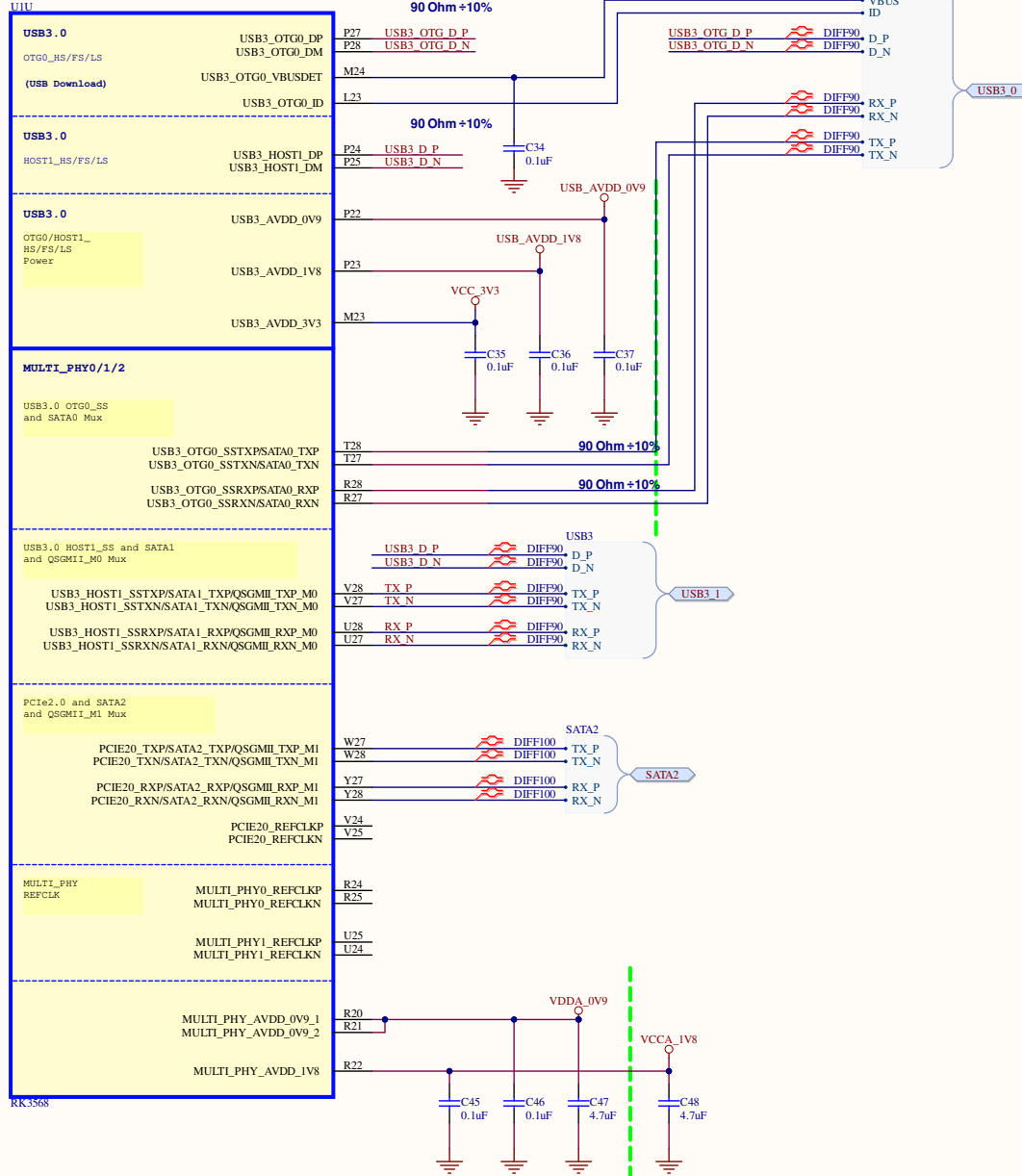
Note:

VCCA_IV8 HW VS R7 91kF R8 8k2F

HW VS	0	1	2	3	4	5	6	7	8	9	10	11	12
ADC Data	0	0	0	0	0	0	0	0	0	0	0	0	0
Full up	X	0	0	0	0	0	0	0	0	0	0	0	0
Full down	100	0	0	0	0	0	0	0	0	0	0	0	0
Resolution		P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7	P1.8	P1.9		

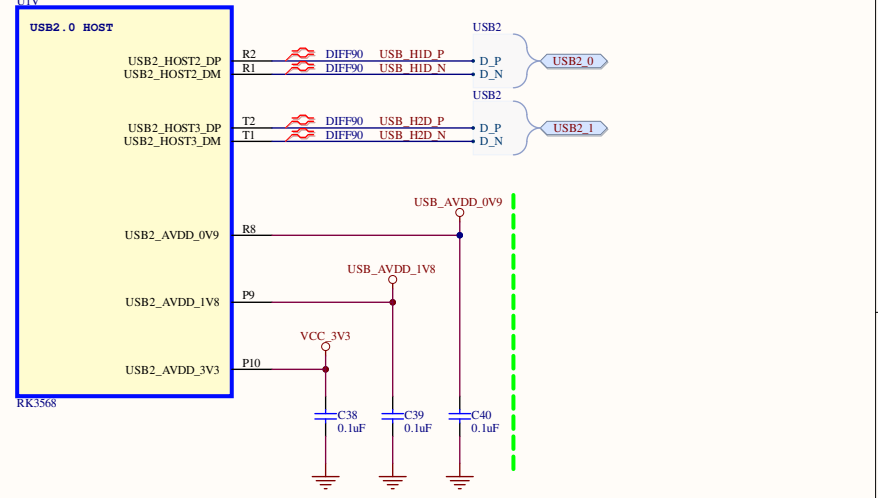
Note: Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_U (USB3.0/SATA/QSGMII/PCIe2.0 x1)

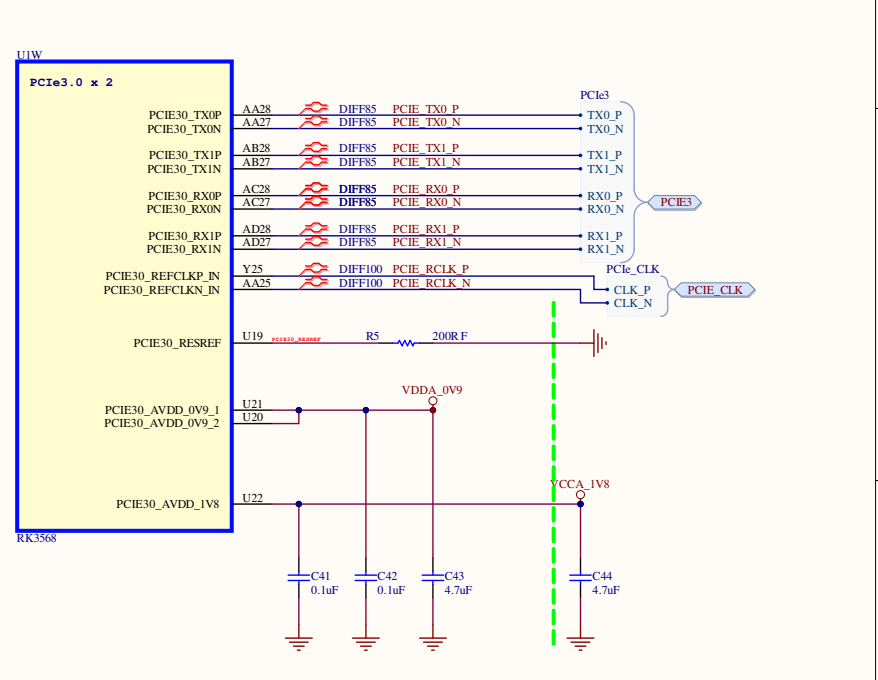


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

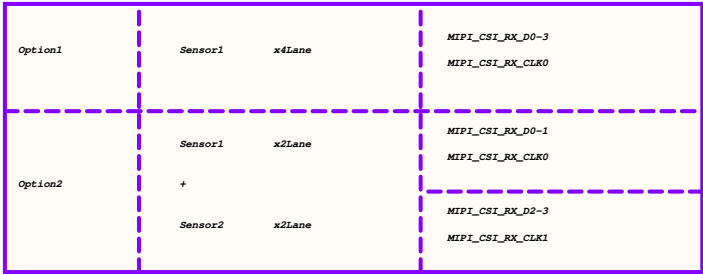
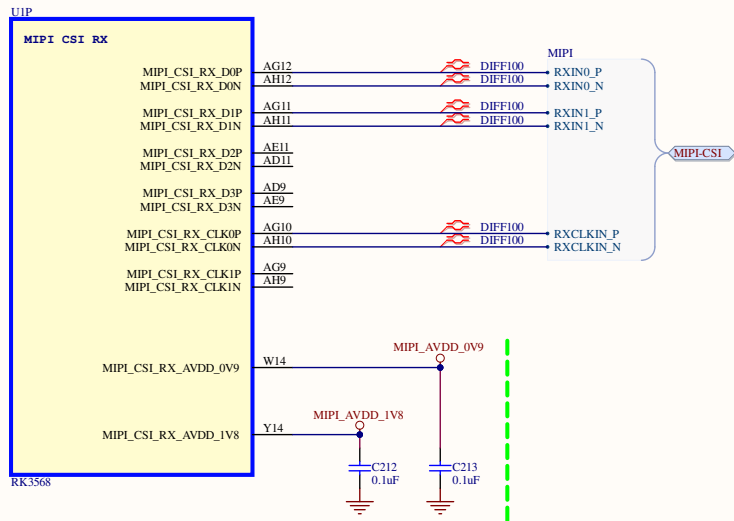
RK3568_V (USB2.0 HOST)



RK3568_W (PCIe3.0 x2)

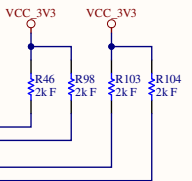
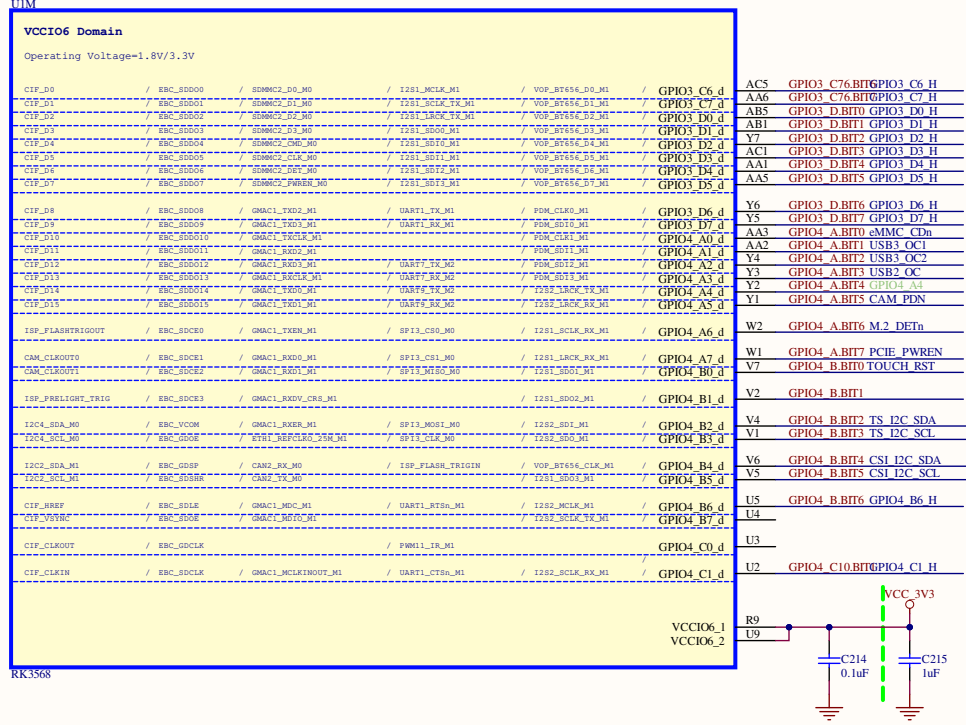


RK3568_P (MIPI_CSI_RX)



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	---	---	---
CIF_D1	D1	---	---	---
CIF_D2	D2	---	---	---
CIF_D3	D3	---	---	---
CIF_D4	D4	D0	---	---
CIF_D5	D5	D1	---	---
CIF_D6	D6	D2	D0	---
CIF_D7	D7	D3	D1	---
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

RK3568_M (VCCIO6 Domain)

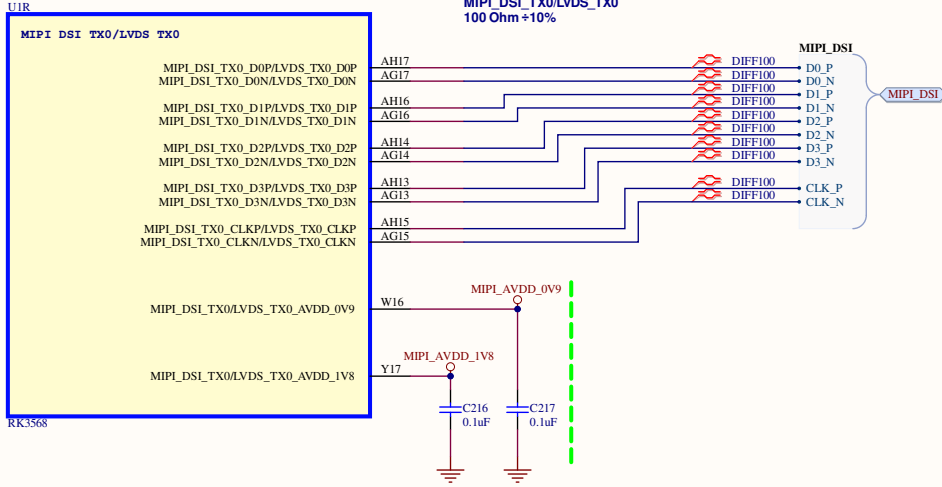


Support BT601 YCbCr 422 8bit input
 Support BT656 YCbCr 422 8bit input
 Support RAW 8/10/12bit input
 Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
 Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

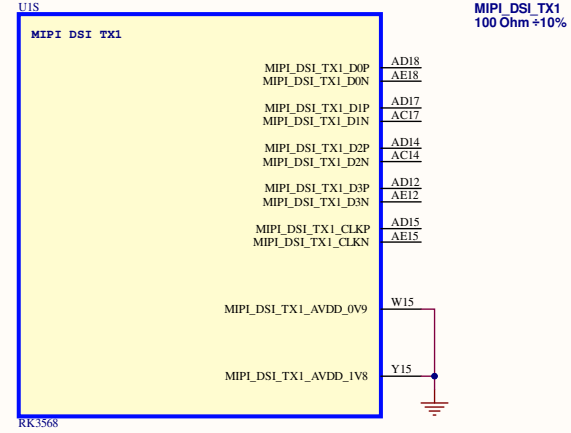
Note:
 Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



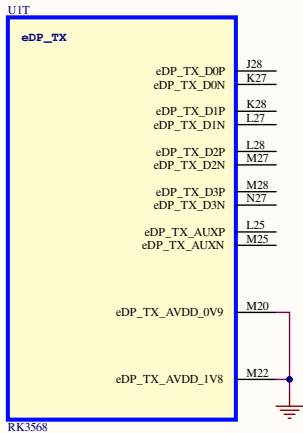
RK3568_R (MIPI_DSI_TX0/LVDS_TX0)



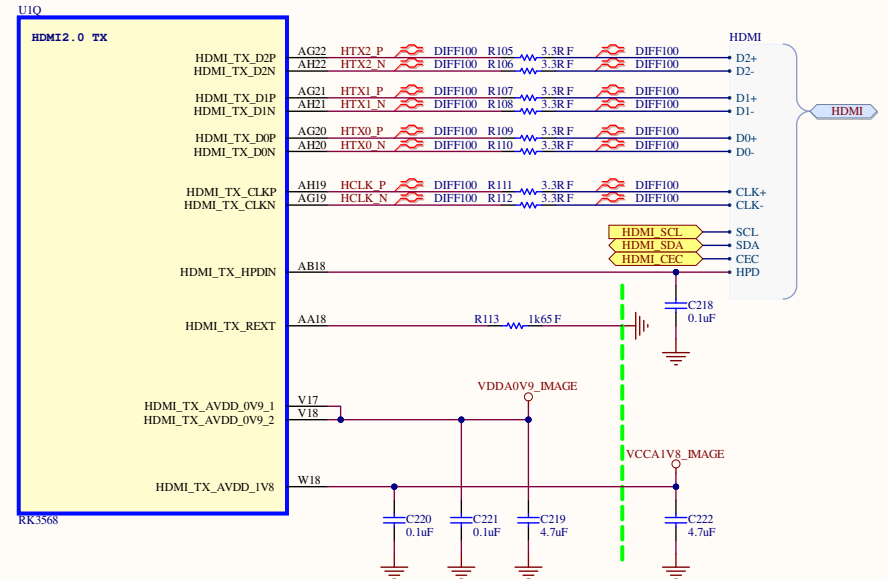
RK3568_S (MIPI_DSI_TX1)



RK3568_T (eDP/DP TX)



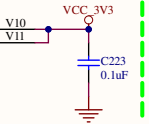
RK3568_Q (HDMI2.0 TX)



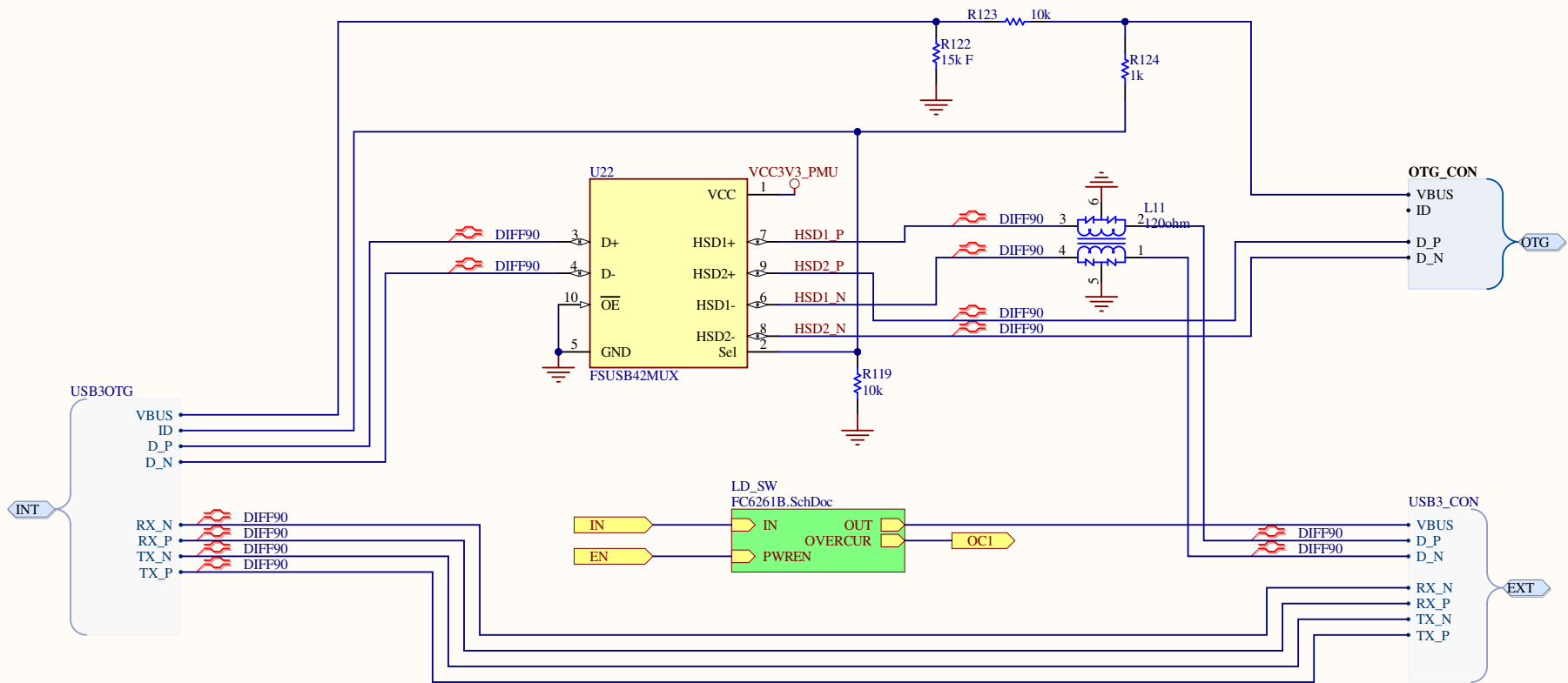
Title RK3568_VO Interface1			Hardkernel Co., LTD. 473-1 Manannu Mananagu, Anyang City Gyeonggdo South Korea		ODROID
Size: A3	Number: 1.	Revision: 0.1	Designed by: ruppi.kim@hardkernel.com		
Date: 2022-01-25	Time: 2:44:25 PM	Sheet 37 of 42			
File: RK3568_VOINTERFACE1.SchDoc					

RK3568_L (VCCIO5 Domain)

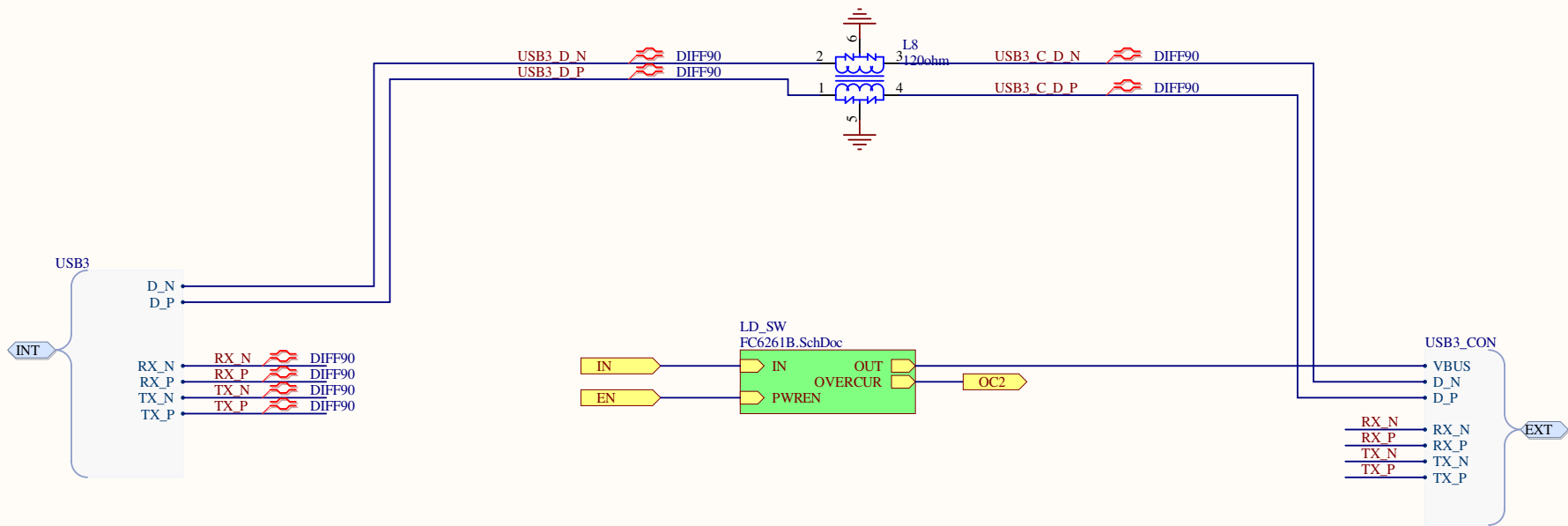
VCCIO5 Domain										
Operating Voltage=1.8V/3.3V										
LDC0_D0	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d	AG6	GPIO2_D.BIT0	GPIO2_D0_H		
LDC0_D1	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D1_d	AD7	GPIO2_D.BIT1	GPIO2_D1_H		
LDC0_D2	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D2_d	AC8	GPIO2_D.BIT2	GPIO2_D2_H		
LDC0_D3	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D3_d	AF5	GPIO2_D.BIT4	PCIE3_CLKREQ0n		
LDC0_D4	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D4_d	AF6	GPIO2_D.BIT5	GPIO2_D3		
LDC0_D5	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D5_d	AD6	GPIO2_D.BIT6	PCIE3_PERSTn		
LDC0_D6	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D6_d	AH5	GPIO2_D.BIT7	GPIO2_D7		
LDC0_D7	/ VOP_BT456_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQ0_M1	/ I2S1_MCLK_M2	GPIO2_D7_d					
LDC0_CLK	/ VOP_BT456_CLK_M0	/ SPI2_CLK_M1	/ UART6_RX_M1	/ I2S1_SDO1_M2	GPIO3_A0_d	AH4				
LDC0_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	GPIO3_A1_d	AB8				
LDC0_D9	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A2_d	AE5				
LDC0_D10	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A3_d	AG4				
LDC0_D11	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A4_d	AF4				
LDC0_D12	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A5_d	AG3				
LDC0_D13	/ VOP_BT1120_CLK	/ GMAC1_TX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A6_d	AH2				
LDC0_D14	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_A7_d	AG2	GPIO3_B.BIT0	GPIO3_B0		
LDC0_D15	/ VOP_BT1120_D0	/ GMAC1_RX0_M0	/ I2S0_SDO1_M2	/ SDMMC2_D0_M1	GPIO3_B0_d					
LDC0_D16	/ VOP_BT1120_D7	/ GMAC1_RX00_M0	/ UART4_RX_M1	/ PWR0_M0	GPIO3_B1_d	AG1	GPIO3_B.BIT1	GPIO3_B1_H		
LDC0_D17	/ VOP_BT1120_D7	/ GMAC1_RX01_M0	/ UART4_RX_M1	/ PWR0_M0	GPIO3_B2_d	AF2	GPIO3_B.BIT2	GPIO3_B2_H		
LDC0_D18	/ VOP_BT1120_D7	/ GMAC1_RX0V_CRS_M0	/ I2S0_SDO1_M2	/ PWR0_M0	GPIO3_B3_d	AF1	GPIO3_B.BIT3	GPIO3_B3		
LDC0_D19	/ VOP_BT1120_D7	/ GMAC1_RX0C_M0	/ I2S0_SDO1_M2	/ PWR0_M0	GPIO3_B4_d	AE1	GPIO3_B.BIT4	GPIO3_B4		
LDC0_D20	/ VOP_BT1120_D7	/ GMAC1_RX0E_M0	/ I2S0_SDO1_M2	/ PWR0_M0	GPIO3_B5_d	AE2	GPIO3_B.BIT5	GPIO3_B5_H		
LDC0_D21	/ VOP_BT1120_D7	/ GMAC1_RX0F_M0	/ I2S0_SDO1_M2	/ PWR0_M0	GPIO3_B6_d	AE3	GPIO3_B.BIT6	GPIO3_B6_H		
LDC0_D22	/ PWR0_M0	/ GMAC1_TX0C_M0	/ UART3_TX_M1	/ PWR0_M0	GPIO3_B7_d	AD4	GPIO3_B.BIT7	GMAC0_nRST		
LDC0_D23	/ PWR0_M0	/ GMAC1_TX0E_M0	/ UART3_TX_M1	/ PWR0_M0	GPIO3_C0_d	AD2	GPIO3_C.S0.BIT0	GPIO3_C0		
LDC0_nBVC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE30_X1_PERSTn_M1	/ I2S1_SDO2_M2	GPIO3_C1_d	AD1	GPIO3_C.S0.BIT1	GPIO3_C1		
LDC0_nBVC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE30_X1_PERSTn_M1	/ I2S1_SDO2_M2	GPIO3_C2_d	AA7	GPIO3_C.S0.BIT2	GPIO3_C2		
LDC0_nBVC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE30_X1_PERSTn_M1	/ I2S1_SDO2_M2	GPIO3_C3_d	AC4	GPIO3_C.S0.BIT3	GPIO3_C3		
PWR04_M0	/ VOP_PWR0_M1	/ GMAC1_MD0C_M0	/ UART7_TX_M1	/ PWR0_CLK1_M2	GPIO3_C4_d	AC3	GPIO3_C.S0.BIT4	GPIO3_C4		
PWR05_CLK_M0	/ PWR05_CLK_M0	/ GMAC1_MD0E_M0	/ UART7_TX_M1	/ I2S1_SDO2_M2	GPIO3_C5_d	AC2	GPIO3_C.S0.BIT5	GPIO3_C5		



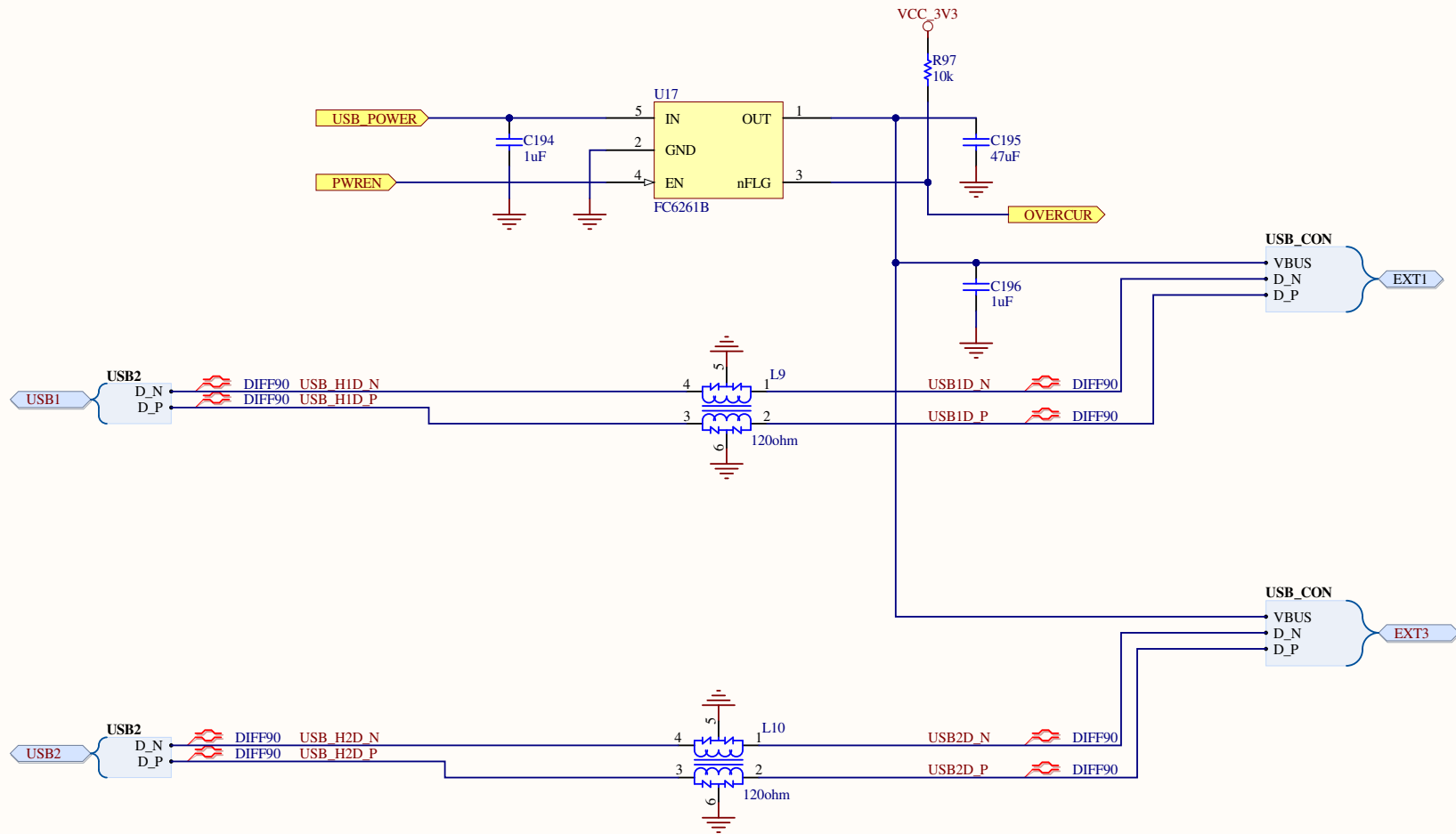
Note:
Caps between dashed green lines and U1000 should be placed under the U1000 package




Title USB3 BUS POWER			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 19.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:25 PM	Sheet 39 of 42		
File: USB3_BUS_PWR2.SchDoc				

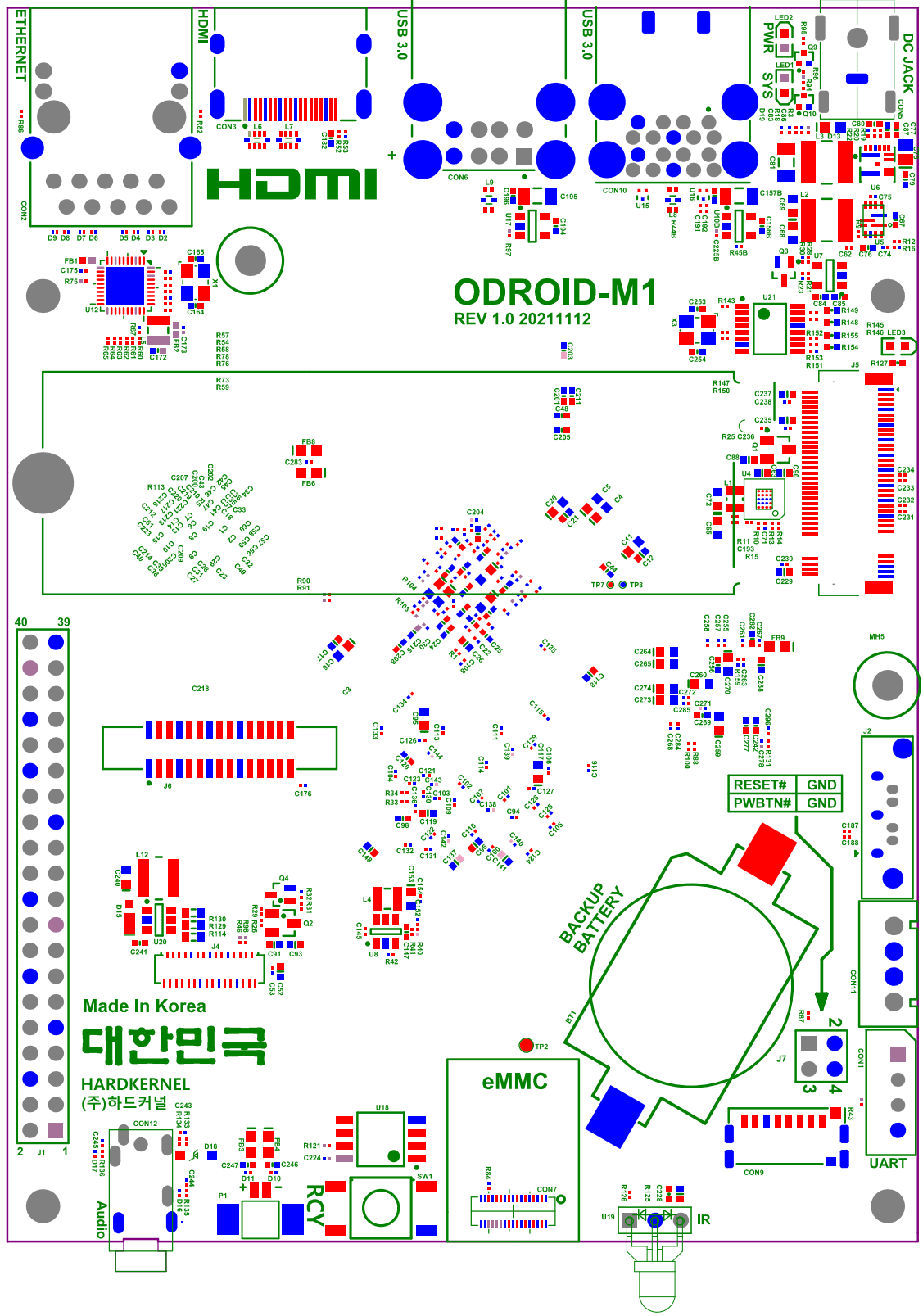


Title USB3 BUS POWER			Hardkernel Co.,LTD. 475-1 Mananro Manangu, Anyang City Gyeonggido South Korea	ODROID
Size: A4	Number: 19.	Revision: 0.1	Designed by: ruppi kim@hardkernel.com	
Date: 2022-01-25	Time: 2:44:25 PM	Sheet 40 of 42		
File: USB3_BUS_PWR.SchDoc				



Title USB HOST PWR SW			Hardkernel Co.,LTD. 1-605 Shinan Metrokhan 1115 Dalandong, Dongangu, Anyang, Gyeonggido South Korea	
Size: A4	Number: 13.	Revision: 0.3		
Date: 2022-01-25	Time: 2:44:25 PM	Sheet 41 of 42		
File: USB_HOST_PWR_SW.SchDoc			Designed by: ruppi.kim@hardkernel.com	

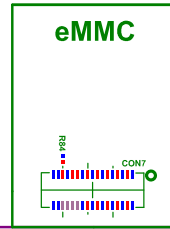
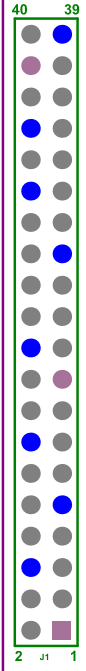
HW REVISION	DATE	Change Note
v1.0	2021.11.10	1. The Mass Production first revision.



ODROID-M1
REV 1.0 20211112

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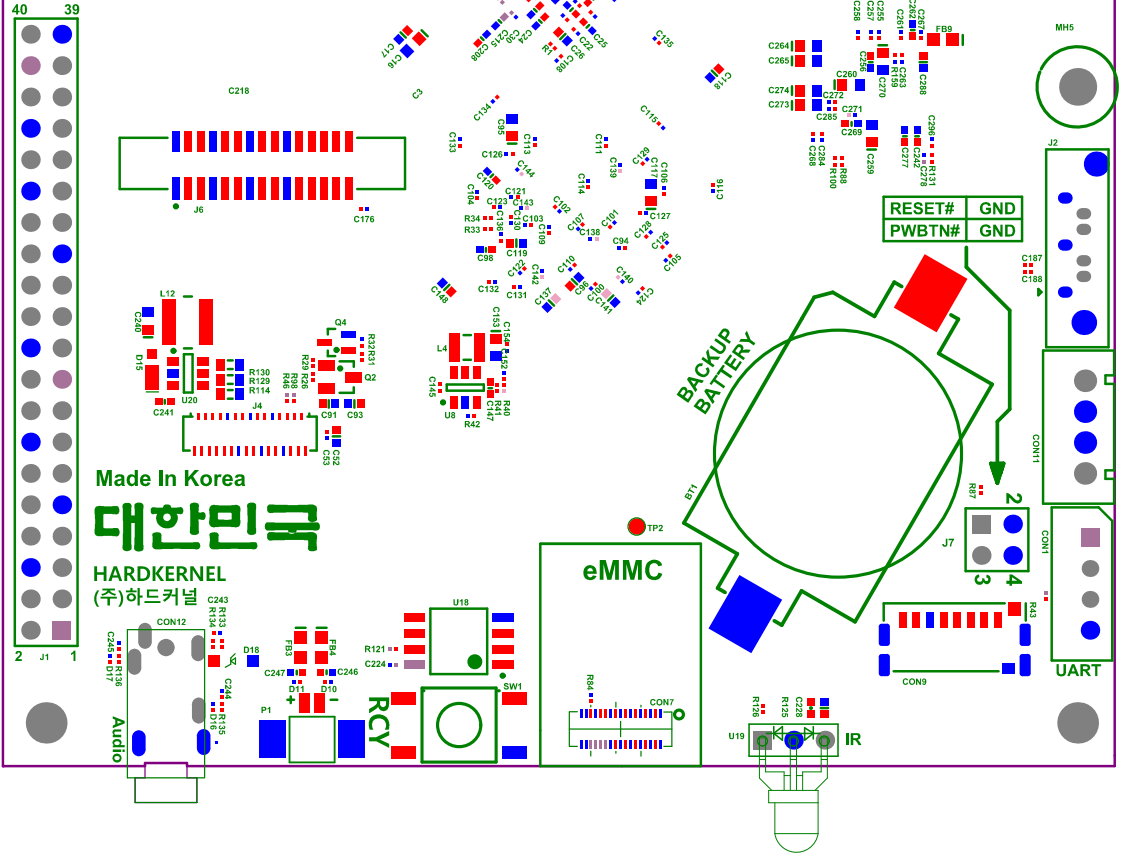
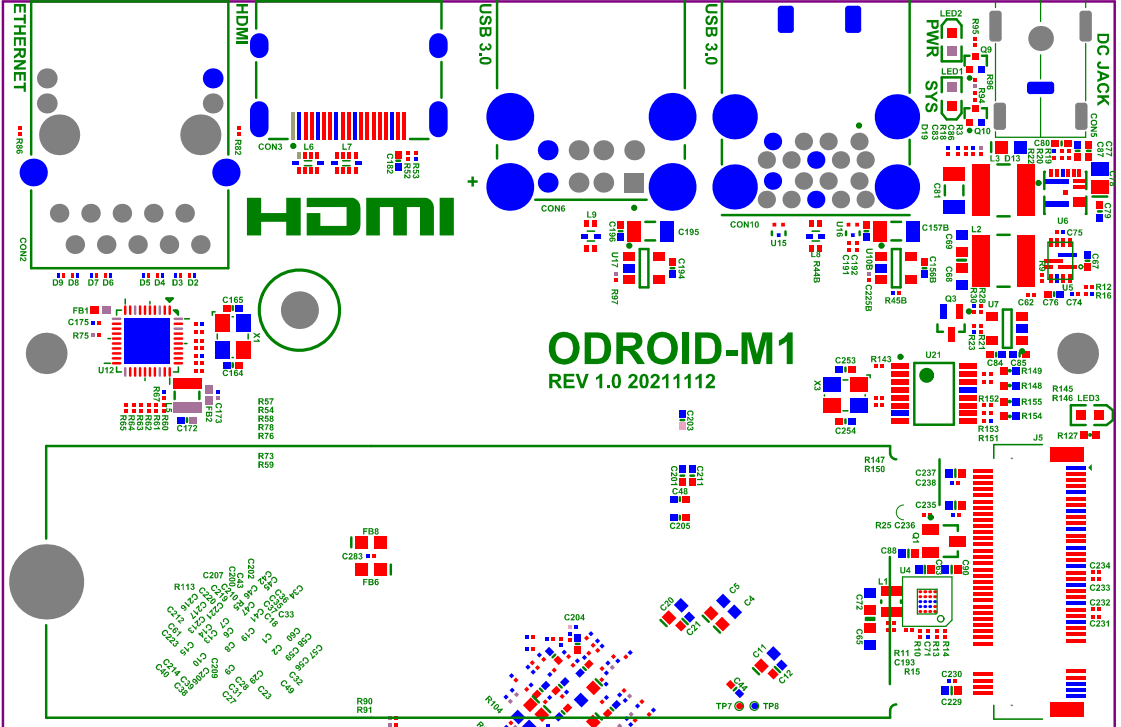
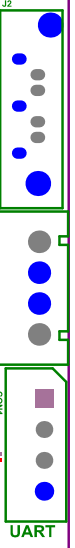


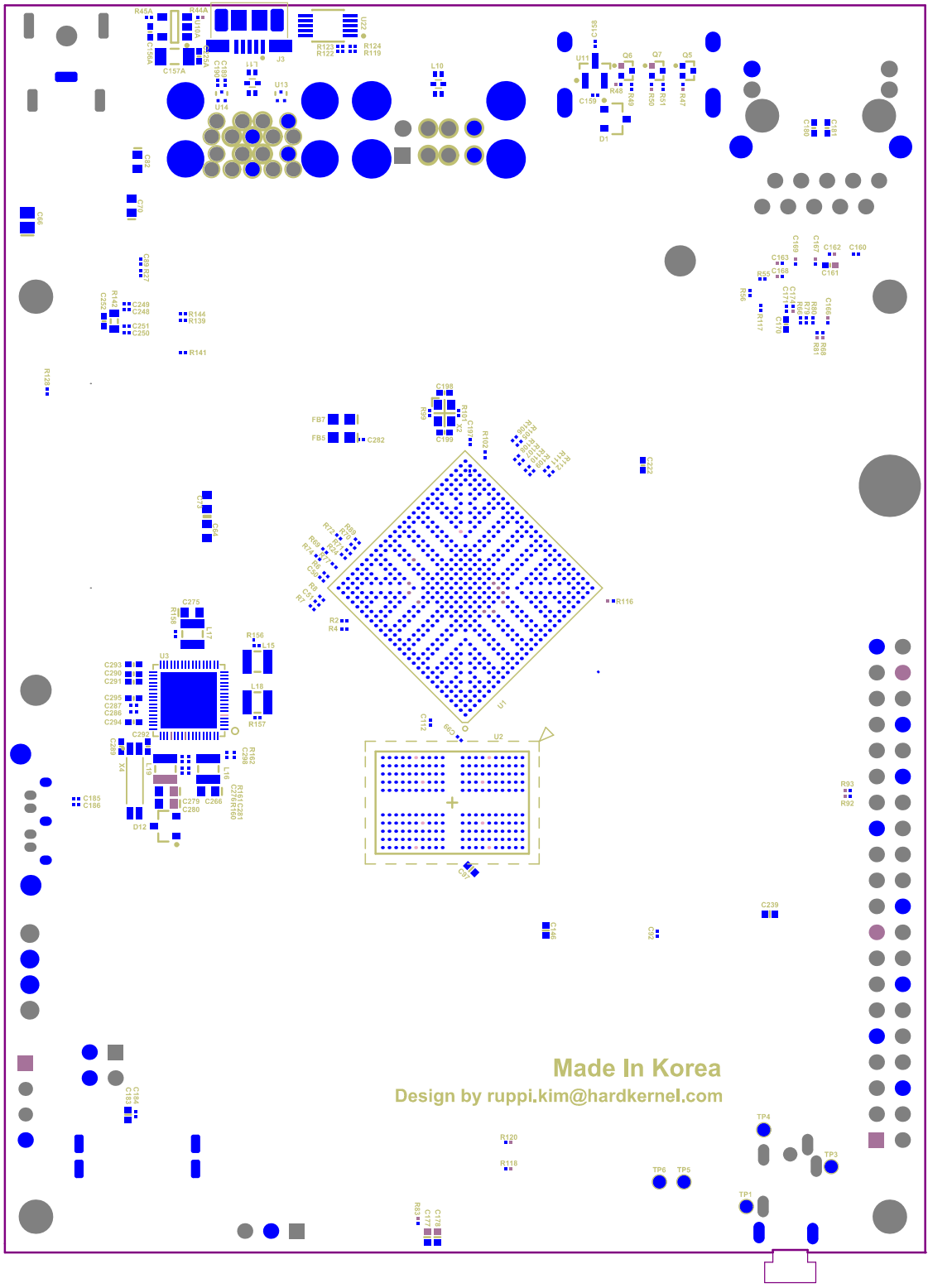
BACKUP BATTERY

Audio

RCY

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